IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-7, Special Issue-10, May 2019 E-ISSN: 2347-2693

Design and Implementation of Low Power and Area Efficient 4 Bit ALU Using MGDI Technique

Nitin Singh

Electronics & Comm. Engineering Dept, Shri Ram Group of Institutions, R.G.P.V Bhopal, India

Corresponding Author: nitinsimps@gmail.com, Tel.: +91-9669918948

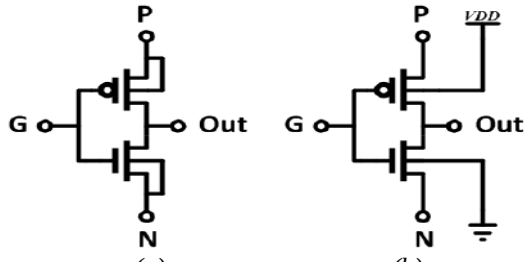
DOI: https://doi.org/10.26438/ijcse/v7si10.8790 | Available online at: www.ijcseonline.org

***Abstract*—** In this paper, the design of a 4-Bit Arithmetic Logic Unit (ALU) using Modified Gate Diffusion Input technique is being done which is implemented using minimum transistor full adder and also adapts hardware reuse method which has advantages of minimum transistors requirement, more switching speed and low power consumption with respect to the conventional CMOS techniques. 4-Bit Arithmetic Logic Unit (ALU) is being implemented with MGDI technique in DSCH 3.5 and layout generated in Microwind tool. The Simulation is done using 65 nm technology at 1.2 v supply voltage The results show that the proposed design consume less power uses less number of transistors, while achieving full swing operation compared to previous work

***Keywords*—** MGDI, PTL, CMOS, Switching Delay, Power dissipation

I. INTRODUCTION

The ALU is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. The processors found inside modern CPUs and Graphics Processing Units (GPUs) have inside them very powerful ALUs. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less. Power consumption of whole data path can be reduced by reducing power consumption of ALU. Adder is the basic building block for an ALU. We have designed ALU by using multiplexer and full adder circuit using MGDI Technique which was first proposed by Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish [1] this technique allows implementation of various complex logic functions using only two transistors as listed in Table I. The original GDI was based on using a simple cell, as shown in figure 1



(a) *(b)*

Figure.1.(a)Basic GDI cell (b) standard CMOS compatible

Table 1. Logic Functions Realization Using GDI Cell.

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
0	1	A	$\bar{}$	NOT

However, it was proposed for fabrication in twin-well MOS or silicon on insulator (SOI) processes, it allowed improvement in power consumption, delay and area of digital circuits compared to CMOS and PTL techniques. The drawback in GDI cell was it suffered from reduced voltage swing due to threshold drops, which leads to performance degradation and increasing static power dissipation. To improve the output of the GDI cells Morgenshtein et al. [2] Proposed the Modified-GDI approach, shown in Fig. 1 (b) where the substrate terminals of NMOS and PMOS transistors connected permanently to GND and VDD, respectively. This modification enables fabrication of GDI cell in standard CMOS processes which is cost efficient compared to twin well and (SOI) processes.

In the present work, the design of a 4 bit Arithmetic And Logic Unit (ALU) using Modified Gate diffusion input technique and Full Adder block is presented and results are compared with that of previous work. The functionality and performance is analyzed using DSCH and Microwind Software tool. Since Microwind integrates front-end and

back-end design into an integrated flow, improving the design cycle and minimizing design complexities. It firmly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification. Performance parameters like area, power dissipation and propagation delay for the ALU's are analyzed at 65 nm using 6metal layer CMOS technology,DSCH and Microwind Software tool.

II. ARITHMETIC LOGIC UNIT

In this paper the MGDI technique is used to realize the circuits. Components required to design the ALU as follows:

A. 2x1 Multiplexer

A multiplexer is a digital switch which chooses the output from several inputs based on a select signal [4], shown in Figure 2 a 2x1 multiplexer consists of 2 transistors.

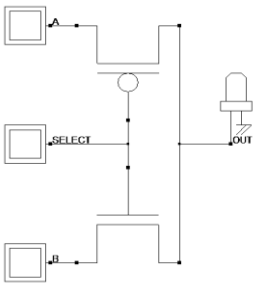


Figure 2. MGDI Based 2x1 Multiplexer

B. 4x1 Multiplexer

Using the previously discussed 2x1 multiplexer a 4x1 multiplexer is realized as shown in Figure 3 it consists of only 6 transistors.

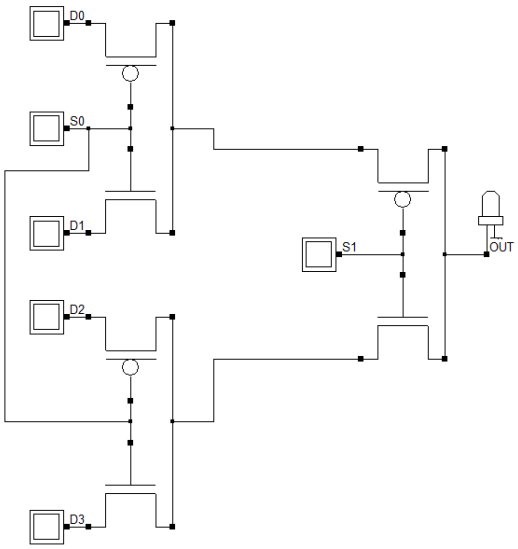


Figure 3. MGDI GDI 4x1 Multiplexer

C. Full Adder

A full adder is a combinational circuit that performs the arithmetic sum of three input bits. It consists of three inputs and two outputs. The adder cell used in this design realized using full-swing AND, OR, and XOR gates. This design was has low power operation, it has the lowest delay and with some modifications it performs the logic operations such as AND,OR,XOR, & XNOR as well, these modifications will save large area of the ALU design.

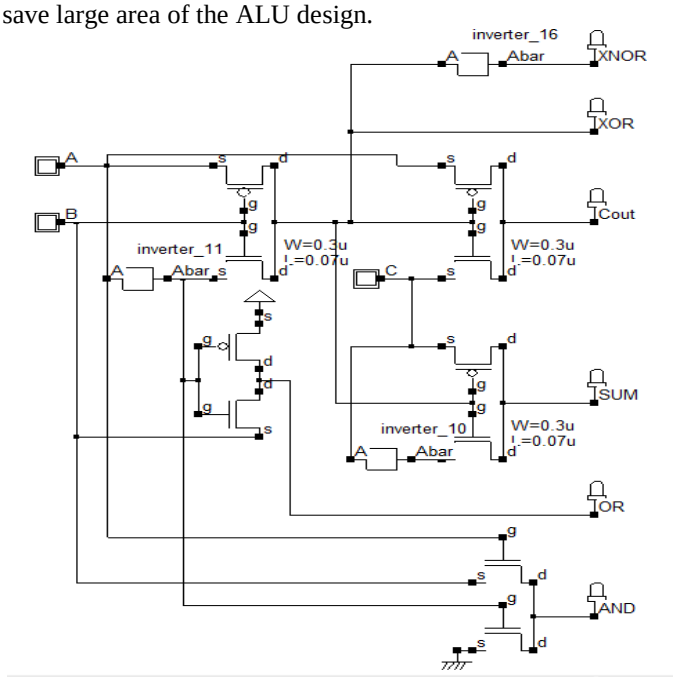


Figure 4. Full Adder cell for ALU

D. Design of Arithmetic Logic Unit

An ALU is a critical component in the Central Processing Unit (CPU) of any computer; even the simplest microprocessors contain one. It performs arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and XNOR [6]. The proposed design of the 4-Bit Arithmetic Logic Unit consists of 4 stages, each stage is an 1-Bit ALU block realized using the previously designed circuits as follows:

Each 1-Bit ALU stage consists of two 2x1 multiplexers, two 4x1 multiplexers and one full adder cell, this design requires 48 transistors as depicted in Fig. 5. Any desired operation can be performed based on the selection line S0, S1, S2 code; Table II summarizes the truth table of the proposed ALU.

Table 2. Truth Table of The Proposed 4-Bit ALU

S2	S1	S0	Operations
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

The 4x1 multiplexer at the input is responsible for the selection of B input based on the values of S0 and S1 selection lines it selects from logic 1, B, B' And logic 0 to perform the Decrement, Addition, Subtraction and the Increment operations respectively, S2 chooses between the arithmetic and the logic operations.

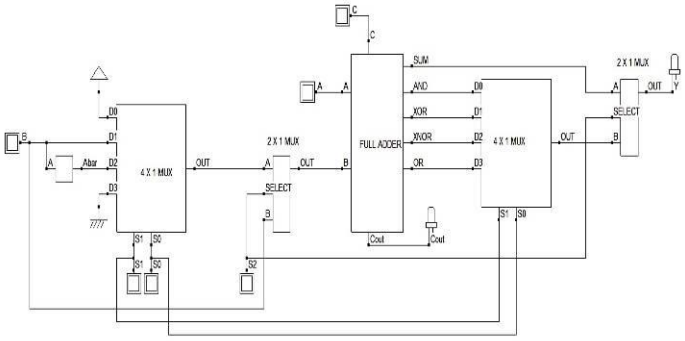


Figure 5. Schematic of 1-Bit ALU Stage

To realize the 4-Bit ALU , four stages were used as shown in Figure 6. While the carry input of ALU0 connected to selection line S1 to obtain logic 1 which needed for subtraction and increment operations, however the other values don't affect the results of the logic operations

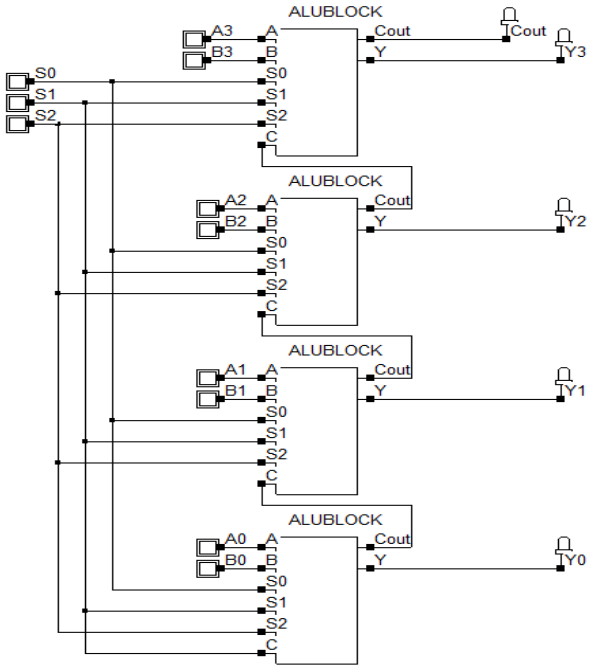


Figure 6. Proposed 4-Bit ALU Design

III. SIMULATION RESULTS AND COMPARISON

The proposed 4-Bit ALU circuits were designed using 65nm CMOS Layout Design Rules, the size of PMOS is(W: 0.5um,L: 0.07um) and that of the NMOS is (W: 0.3um,L: 0.07um) to achieve the best power and delay performance. The simulations were done using the WinSPICE based DSCH & Microwind simulator with a power supply of 1V. Using A,B,C as test inputs and S2,S1,S0 as select input Figure 7 shows the waveform of the proposed ALU, The results of the proposed design compared with the 4-Bit ALU designs in [5], [6], [7] are shown in Table III. Among these designs the proposed ALU design outperforms in terms of power consumption and transistor count. In respect of power consumption the proposed ALU operates at least values. Compared with the other designs the Transistor count is also reduced.

Table 3. Simulation Results Of The 4-Bit ALU Designs

Design	Technology	No. of Transistors	Power (µW)
Vivechana [5]	250nm	232	1030.5 µW
G.Sree Reddy [6]	120 nm	232	543.24 µW
S. Usha [7]	180 nm	88	2225 µW
M.A. Ahmed [8]	65 nm	192	24.01 µW
Proposed Design	65 nm	136	112.02 µW

IV. CONCLUSION

This work presents a 4-Bit ALU designed in 65nm CMOS Design using the MGDI technique and simulated using the DSCH & Microwind simulator. Simulation results showed an advantage of the proposed ALU design in terms of power consumption and transistor count, while maintaining Full-Swing Operation. The proposed design consists of 136 transistors and operates under 1V supply voltage.

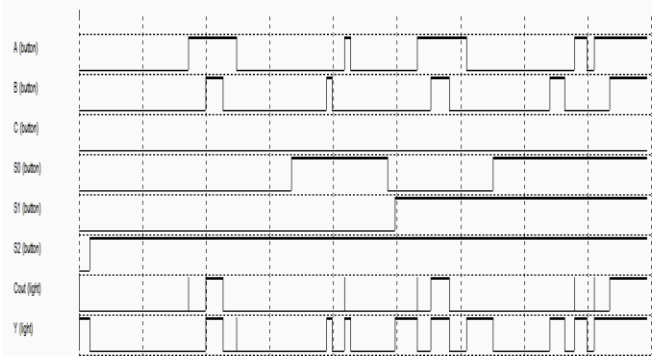


Fig. 7. Waveform of the Proposed 4-Bit ALU

REFERENCES

[1] A. Morgenshtein, A. Fish, and I. Wagner, "Gate-diffusion input (GDI):a power-efficient method for digital combinatorial circuits," IEEETransactions on Very Large Scale Integration (VLSI) Systems IEEE Trans.VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

[2] A. Morgenshtein, I. Shwartz, and A. Fish, "Gate Diffusion Input (GDI)logic in standard CMOS Nanoscale process," 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.

[3] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.
[4] N. Weste, D. Harris, CMOS VLSI Design a Circuits and Systems Perspective, 4th Ed, Addison-Wesley, 2011.
[5] M. Shoba, R. Nakkeeran, "GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, vol. 19, no. 1, pp. 485–496, Mar. 2016
[6] Chandra Srinivasan, "Arithmetic Logic Unit (ALU) Design Using Reconfigurable CMOS Logic," M.S. Thesis, Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, LA, USA 2003.
[7] Vivechana Dubey, Ravimohan Sairam, "An Arithmetic and Logic Unit Optimized for Area and power" IEEE Fourth International Conference on Advanced Computing & Communication Technologies.,pp.330-334, 2014.
[8] G. Sree Reddy, K. V. Koteswara Rao,"32-Bit Arithmetic and Logic Unit Design With Optimized Area and Less Power Consumption By Using GDI Technique" International Journal of Research In Computer Applications and Robotics, Vol.3 Issue.4, pp. 51-66, April 2015.
[9] S. Usha, M. Rajendiran, A. Kavitha, "Low Power Area Efficient ALU With Low Power Full Adder" IEEE International Conference on Computing for Sustainable Global Development (INDIACom), pp. 1500- 1505, 2016.
[10] Mahmoud Aymen Ahmed, M. A. Abdelghany " Low Power 4-Bit Arithmetic Logic Unit Using Full-Swing GDI Technique ", pp 193-196, 2018.

