IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-7, Special Issue-18, May 2019 E-ISSN: 2347-2693

A Study of the effect of composite dielectric on the switching behaviour of Junction less Transistor

S. Ghosal[1*], A.Sikdar[2], D.Ghosh[3]

[1,2]Dept. of Electronic Science, Acharya Prafulla Chandra College, WBSU, Kolkata, India
[3]Dept of Basic Sc & Humanities, RERF, Kolkata, India

Corresponding Author:habli_g@yahoo.com

Available online at: www.ijcseonline.org

***Abstract*—** The unremitting drive for faster and smaller devices has also imposed stringent technological constraints on the associated silicon technology. An increased sensitivity to variability in process conditions as well as a need for ultra sharp doping profile has led to the search for alternatives to the conventional Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET) . An obvious alternative is a device architecture that does not have any junctions in the source-channel-drain path. Amongst many advanced MOSFET structures, the Junction-less transistor (JLT) is one such structure which mitigates these requirements while reducing short channel effects because of its excellent scalability. For widespread application in today's high-speed circuits a key factor would be its effectiveness as a switch. In this work we have studied the relative sensitivity of transient parameters namely the ION/IOFF ratio and gate capacitance have been calculated to variations in several structural parameters of the device namely channel width and doping concentration of the channel. In order to suppress the gate leakage current with continuous thinning of gate oxide layer, gate oxide with high-k materials are being used as a possible solution in MOSFETs. However high-k materials like HfO2 lead to a degradation in mobility due to surface roughness scattering. Therefore we have studied the effect of SiO2 , HfO2 and a gate stack of same EOT and found the gate stack to give a much improved switching performance.

***Keywords*—**JLT, gate stack, Switching ,ION/IOFF ratio, EOT

I. INTRODUCTION

Traditional downscaling device technologies have served the unremitting drive for faster and smaller devices over the last three decades. Scaling with new materials & new device structures are now continually improving the performance of device technologies [1] .However the need for ultra-sharp junctions between source/drain and channel as we move into the sub-30nm regime poses a severe technological challenge as the doping concentration has to vary by several orders of magnitudes over a span of a few nanometers in order to minimize the possibility of lateral encroachment of source and drain impurities into the channel region. Amongst many advanced MOSFET structures [2-5], the Junction-less transistor (JLT) is one such structure which mitigates the need for ultrsharp gradation by using a uniformly doped channel. Junctionless transistor was firstly created by a team of scientists at the Tyndall National Institute in Cork, Ireland [6-7].It is comprised of an isolated ultra-thin highly-doped. The effectiveness of an electronic device as a switch is determined by a set of key parameters. In this paper we look at two of them. The drain current of a MOSFET is controlled by thermionic emission from the source into the channel. As the gate voltage increases, the potential barrier between the source and the channel decreases, leading to an increase in the drain current. This leads to two problems – a larger OFF-state current due to subthreshold conduction and a higher subthreshold slope. The ION/IOFF ratio one of the key factors determining the effectiveness of such nano-scale devices as a switch. Another factor of critical importance is the parasitic gate capacitance. The values of the capacitances are determined by the structure of the device, the materials involved, and by the voltages across them. The gate-to-source capacitances impact the susceptibility of unwanted dv/dt induced turn-on. However, continual gate oxide scaling requires high k gate dielectric; since the gate oxide leakage increases with reduced physical thickness of gate oxide (SiO2).Various materials like HfO2, ZrO2 have device layer that exhibits neither source/drain junctions nor doping concentration gradients.

Proposed as alternatives. In an earlier work [8] have studied the effect of channel concentration and thickness using both SiO2 and HfO2 .However while HfO2 gave better simulation results it has a physical constraint in that the dielectric-Si interface surface roughness leads to a degraded mobility although the effect is less pronounced than MOSFET as it is based on bulk conduction. Nevertheless we have done a comparative study of the effect of a gate stack on the switching behavior of a JLT.

The rest of the paper is organized as follows. A brief introduction to junctionless transistors is given in Section II followed by our simulation results in Section III and conclusion in Section IV.

I. JUNCTIONLESS TRANSISTOR

The need for ultra steep doping profiles has made realization of metallurgical junctions beyond 32nm node for a metal oxide semiconductor field effect transistor (MOSFET) extremely challenging. In 2010 Coolinge et all [9-10] proposed a structure based on the Lilienfeld's first transistor architecture which does not have any metallurgical junctions.

The schematic representation of double gate junctionless transistor is shown in Fig. 1.As shown the structure consists of a uniformly doped semiconducting silicon bar with no separate source or drain region. For an n-channel operation, the source, channel and drain are of n-type doping and the gate is of a p-type. Since the work function difference between the n-type channel and the p-type gate determines the depletion in the channel, the channel can be made fully depleted by choosing an extremely thin channel and channel doping in the range of 10nm and 1E+19 respectively. Once the channel is fully depleted, the current between the source and drain becomes very small. Gate bias needs to be applied to bring the channel out of depletion and enable conduction between source and drain. At the threshold voltage the peak electron concentration in the channel reaches the doping concentration ND.

The structure may be modelled as a semiconductor resistor with uniform doping from the source to channel, whose resistance can by modulated by the gate. However, for a reasonable conductance between source and drain, the doping of the semi-conductor bar needs to be very high.

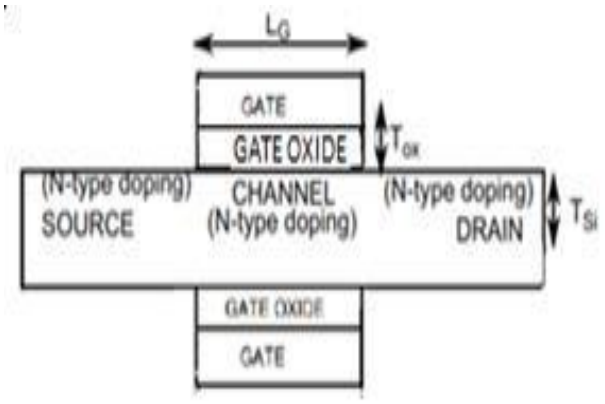

Figure 1. Schematic of a double gate Junctionless Transistor.

Besides the obvious advantage with regard to fabrication of a simpler structure without ultra-sharp junctions the potential benefits of this structure are manifold.

The lateral extension of the S/D depletion charges in the channel region responsible for short-channel effects such as DIBL and degraded subthreshold slope are absent in a JLT. The current drive is controlled by doping concentration and not by gate capacitance. Moreover due to zero doping gradients, no diffusion take place from source to drain. The junction less device uses bulk conduction instead of surface channel conduction lowering the possibility of mobility degradation due to surface scattering associated with use of high-k dielectrics.

II. METHODOLOGY

The laws of diffusion and the statistical nature of the distribution of the doping atoms, makes nanoscale devices with high doping densities highly susceptible to variability in process conditions. Inevitably there is variability in the doping profile and device dimensions at the nano-level in both vertical and horizontal direction. In an earlier project we have made a simulation study [8] of the sensitivity of the switching property of the JLT namely ION/IOFF ratio by varying various parameters of the device. We have also plotted variation of parasitic Gate capacitances for a frequency of 1E9 Hz. The value of Cgd determines the susceptibility of a device to dv/dt induced turn-on. These two capacitances which constitute the input capacitance. must be charged to the threshold voltage before the device begins to turn on, and discharged to the plateau voltage before the device turns off. Therefore, the impedance of the drive circuitry and Ciss have a direct effect on the turn on and turn off delays. In order to estimate the transient performance, analysis of various transient characteristics such as intrinsic gate delay , unity-gain cutoff frequency and gain bandwidth product (GBW) have been calculated.

However the use of HfO2 leads to a degradation in mobility due to interface roughness. In order to highlight the effect of High K dielectric we have in an earlier work [8] simulated the parameter variations for both SiO2 and HfO2. To combine the advantages of gate and channel engineering we have used a gate stack which has ealier been used for MOSFET..The lower layer is SiO2 while the top layer is HfO2 .The high-κ oxide layer helps in overcoming the leakage and scaling problems while SiO2 provides the inter-face stability and mitigates the fringing fields.It can be observed that that the high-κ dielectric (HfO2+ SiO2) gate stack increases the surface potential than a low-κ dielectric (SiO2), implying higher gate capacitance and reduced gate leakage current while assuring small capacitive coupling than high-κ gate dielectric (HfO2).

In each of the simulations one of the structures is chosen as the control and its work function is adjusted to achieve the targeted OFF state leakage current of 1E-7.Aμm-1 as per the ITRS roadmap [1], while the saturation current at Vg=1.2V is taken as the ON current. [12]

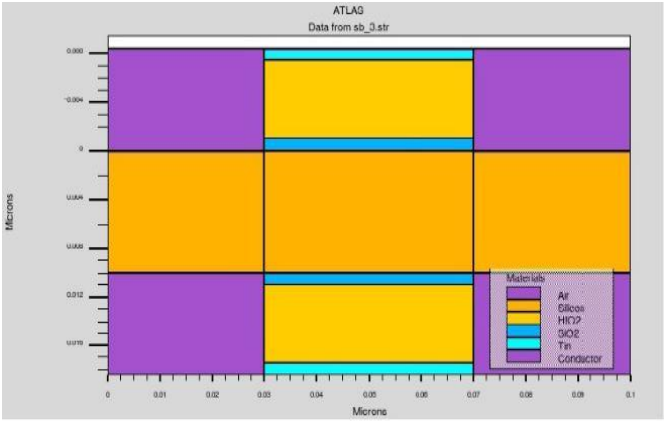

Figure 2. Structure of JLT used in our simulation study

For the other structures the current at Vg =0 is taken as the OFF current. The threshold voltage is the gate voltage at which I D =5E-6 Aμm-1 as per the ITRS roadmap for a gate length of 40 nm.

For this study we used a double gate structure (Fig. 2) with a gate length of 40 nm and an effective oxide thickness (EOT) of 2 nm. In each case the effective oxide thickness is 1.nm. The thickness of SiO2 and equivalent HfO2 are 1nm, 6.41nm respectively. To get equivalent thickness of the high-k as 6.41nm, the physical thickness is calculated according to EOT =TK (KSiO2 /KHIGH K) , where Tk is the physical thickness of high-k, k is the permittivity of dielectric material . The work function for the gate electrode is assumed as 4.8ev.

III. RESULT AND DISCUSSION

A. Channel Thickness

For the junctionless transistor the channel thickness is a critical parameter, a too thick channel will prevent a complete pinch off in the OFF state while a thinner channel reduces ON current and thereby its drive capability. Here we have studied the effect of channel thickness on the transfer characteristics of a composite dielectric (Fig 3) and compared it to the results obtained for the two dielectrics separately.(Table 1). It is observed that as expected the channel OFF progressively increases as we move towards larger channel widths. Of the two gate-dielectrics, the leakage current was observed [8] to be higher in case of HfO2-TiN than SiO2-polysilicon. It is observed that the sensitivity of current ON/OFF ratio on thickness is much lower for composite diectric as compared to HfO2-TiN and SiO2-Polysilicon..The composite dielectric shows a markedly improved behavior across all channel lengths except at 8 nm. In the subthreshold region ,exponential dependence of the drain current is of the form [13] exp (Vgs/(nVT)) which leads to an expression for subthreshold voltage S=nVT.ln(10) where n=1 + Cb/Cg ; Cb=ϵSi/wd Cg= ϵOX/tOX . Now the higher dielectric constant of HfO2 leads to an increase in oxide capacitance which translates to a lower value of n. The lower value of n leads to a higher leakage current for HfO2 an effect moderated by the composite dielectric.

Thus a higher gate capacitance (owing to higher di-electric constant) leads to a reduced effect of the width-dependent term. The curves show that although there is a marginal increase in the ON current with width the ON/OFF ratio progressively decreases with channel width and for a concentration of 1E19 the channel fails to turn OFF for widths of 11nm and higher. Thus a judicious choice has to be made with respect to the application.The composite dielectric gives the most marked improvement over the other two dielectrics for a channel width of 10nm which is the optimum width with respect to OFF current.The capacitive switching behavior increases monotonically with reduction channel widths.The nature of variation is found to be more consistent than with the other two dielectric combinations.

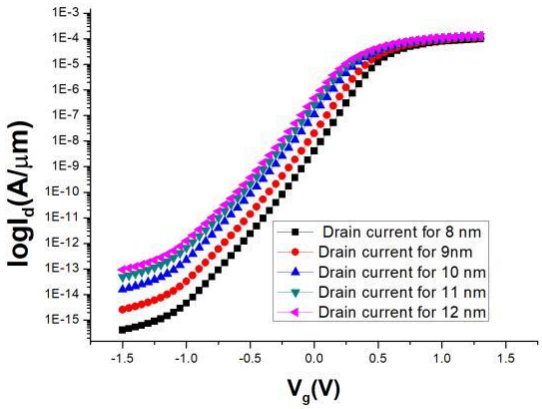

Figure 3. Transfer characteristics for Composite Dielectric with channel thickness variation

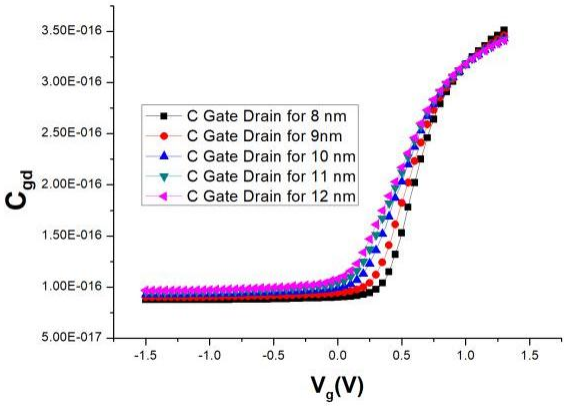

Figure 4. Gate to Drain capacitance for Composite Dielectric

Table 1. ION /IOFF vs Channel thicknessfor SiO2 - Polysilicon and HfO2-TiN

Dielectric	Channel Thickness(nm)				
	8	9	10	11	12
SiO_2/Poly(x10^3)	342	9.4	0.57	0.173	0.027
HfO_2/TiN (x10^3)	59.5	4.52	0.333	0.039	0.008
Composite Dielectric (x10^3)	22.56	5.25	1.054	0.464	0.269

B. Channel Concentration

The next parameter to be varied was channel concentration. Once again, a proper matching of the channel concentration with the gate work-function is required for optimum switching characteristics. We chose a channel concentration of 5E18 as the control structure with an OFF current of 1E-7. The channel concentration was varied over a range 1E+17 to 1E+20 keeping a channel width of 10 nm, gate length 40 nm and the effects on transfer characteristics, threshold voltage and ION /IOFF ratio were respectively observed.

The transfer characteristics show that the channel fails to turn OFF for channel concentrations in excess of 1E+19. The depletion width of the bulk semiconductor i.e channel is inversely proportional to the doping concentration, thus for a given channel width the required voltage to pinch off the channel increases with doping. As we restricted the reverse voltage to 1.3 V in magnitude the device failed to turn OFF. A relative comparison in the subthreshold slope for the different di-electrics under study] that the subthreshold slope is sharper in the case of the High-K dielectric.

From the transfer characteristic, (Fig 5) the following observations are made Variation in threshold voltage with channel concentration is less severe for HfO2-TiN than SiO2-Polysilicon indicating better immunity to process variation. In nano-scale devices a difference of a few dopant atoms due to a statistical variation in the implantation energy may affect a sharp change in the channel doping concentration ; so this immunity for the high K dielectric is a significant avantage. The current ON/OFF ratio decreases sharply with concentration. However while SiO2 dielectric gives a higher ratio ,its sensitivity to doping concentration is also high. Over the studied range the ON current increased from 1E-6 to 1E-3 but the rise in OFF current was significantly higher; hence a tradeoff between the drive capability and switching behaviour has to be made based on the domain of application of the device.In this respect the composite dielectric gate gave its highest ratio for 1E18 but its sensitivity to variation in channel concentration is also much lower indicating a larger tolerance to process induced variability due to random dopant variation(RDD).

The capacitive behaviour as plotted in Fig 6 follows a similar trend.There is a sharp switching activity between the cocentration range of 10E18 to 1E19 indicating the extreme sensitivity of the JLT to channel concentration.The values are marginally higher for SiO2.

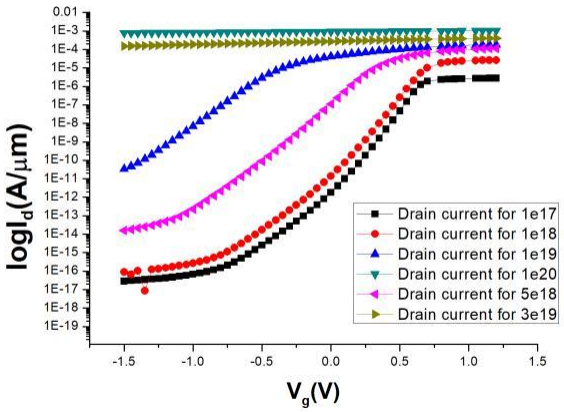

Figure 5. Transfer characteristics for Composite Dielectric with channle thickness variation

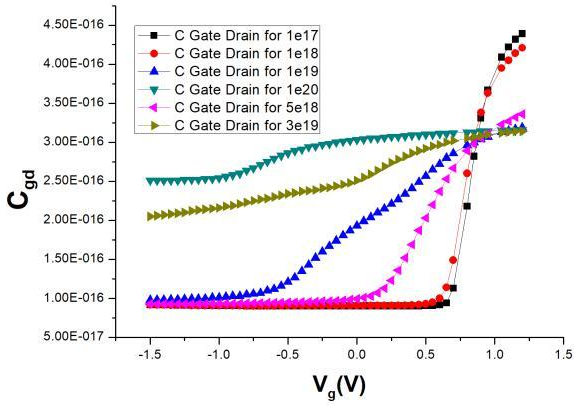

Figure 6. Gate to Drain capacitance for Composite Dielectric

Table 1I. ION /IOFF vs Channel concentration for SiO2 - Polysilicon and HfO2-TiN

Dielectric	Channel Concentration(nm)					
	1E17	1E18	5E18	1E19	3E19	1E20
SiO_2/Poly(x10^3)	3570	3050	2.54	0.005	0.002	.001
HfO_2/TiN (x10^3)	1195	1381	1.12	0.004	0.002	.001
Composite Dielectric(x10^3)	1547	1907	1.05	0.441	.0015	.0011

IV. CONCLUSION AND FUTURE SCOPE

In this work we have tried to study the effect of various structural parameters like channel width, channel doping as well non-uniformity in composition. Our results have clearly demonstrated that use of a composite dielectric (i.e. SiO2 - HfO2) in place of SiO2/HfO 2 leads to a marked

improvement in performance. While use of stack dielectric is present in MOS technology[14] there is not much reported work on use of gate stack in JLT.Creation of high doping concentration in nano-scale devices often leads to a spatial inhomogeneity due to variation in energy during the ion-implantation process[15]. We have attempted to study the effect of such variability in the doping profile for the highly doped channel. We will be studying the effect of this composite dielectric on other parameters critical to transient behavior like intrinsic delay, unity-gain cutoff frequency and gain -bandwidth product. It was observed from the simulation results that while the ION/I OFF ratio was not more than an entirely High K dielectric gate oxide the composite dielectric JLT showed a consistently less variation for both parameters under study making it a promising candidate for a robust variability resistant workhorse for modern electronics.

REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS). Available at hppt://www.itrs.net.

[2] Skotnicki, T., Merckel, G., Pedron, T.: The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects. IEEE Electron Device Lett. 9, 109 (1988).

[3] Scott Thompson, Paul Packan, Mark Bohr "MOS Scaling: Transistor Challenges for the 21st Century" Intel Technology Journal, vol. 2, issue 3, 1998.

[4] C. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, "A Comparative study of advanced MOSFET concepts," IEEE Transactions on Electron Devices, vol. 43, p. 1742, Oct. 1996.

[5] A. Chaudhry, M.J. Kumar, Controlling short-channel effects in deep submicron SOI MOSFETS for improved reliability: a review, IEEE Transaction Device Material Reliability, 4 (3), 99–109, 2004.

[6] S. Barraud, M. Berthomé, R. Coquand, M. Cassé, T. Ernst, M-P. Samson, P. Perreau, K. K. Bourdelle, O. Faynot, and T. Poiroux, "Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm," IEEE Electron Device Lett., vol. 33, no. 9, pp. 1225-1227, Sep. 2012

[7] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nat. Nanotechnol., vol. 5, no. 3, pp. 225–229, Mar. 2010

[8] S Ghosal " A Study on sensitivity of ION/IOFF ratio of JLT to structural parameters " in the Proceedings of the 2018 IEEE Electron Device Kolkata Conference Vol.6(9), Sep 2018, E-ISSN: 2347-2693

[9] J. P. Colinge, C. W. Lee, N. DehdashtiAkhavan, R. Yan, I. Ferain,P. Razavi, A. Kranti and R. Yu "Junctionless Transistors: Physics and Properties" Springer-Verlag Berlin Heidelberg 2011.

[10] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," Appl. Phys. Lett., vol. 96, no. 7, p. 073510, Feb. 2010

[11] Atlas User's Manual by Silvaco International

[12] S.Sil, M.Sil, Mallik A "Comparison of Logic performance of CMOS Circuits implemented with Junctionless and Inversion-Mode Fin-FETs" IEEE Trans. Electron Devices,2017,64(3),pp.953-959.

[13] R.Trevisoli, R.Doria, M.deSouza, Pavanello "Threshold voltage in junctionless nanowire Transistors"SemicondSci.Technol. Vol26 ,no.10,(2011).

[14] J. Zhang, J. S. Yuan, and Y. Ma, "Modeling short channel effect on high-k and stacked-gate MOSFETs," Solid-State Electronics, vol. 44, no. 11, pp.2089 – 2091, 2000.

[15] D. D. Zhao, C. H. Lee, T. Nishimura, K. Nagashio, G. A. Cheng, and A. Toriumi, "Experimental and Analytical Characterization of Dual-Gated Germanium Junctionless p-Channel Metal–Oxide–Semiconductor Field-Effect Transistors," Jpn. J. Appl. Phys., vol. 51, no. 4, pp. 04DA03-1-04DA03-7, Apr. 2012Symposium on Colossal Big Data Analysis and Networking Security, Canada, pp.111-117, 2015.

Authors Profile

Dr. S.Ghosal pursed Bachelor of Science from University of Clacutta, India in 1994 and Master of Science from Calcutta University in year 1996. He completed his Ph.D. from Jadavpur University in 2010 in the field of nanostructure devices. Since 2001 he is working as Assistant Professor in Department of Electronic Science, Acharya Prafulla Cahndra College, West Bengal state University. He has published more than 20 research papers in reputed international journals and conferences including..His current research work focuses on variability issues in nano-structure devices.

Mr A.Sikdar pursed Bachelor of Science and Master of Science from West bengal State University in year 2016 and 2018 respectively. He is currently pursuing Ph.D. on variability issues in . nano-structure devices.

Miss D.Ghosh pursed Bachelor of Science and Master of Science from West bengal State University in year 2014 and 2016 respectively. She is currently working as Assistant Professor in Regent Education and Research Foundation.. She is also pursuing her Ph.D. on variability issues in nano-structure devices

