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An alternative approach to realize all optical frequency encoded integrated AND-OR logic gate with control input using optical switches and its simulative verification.

B. Ghosh[1], N. Halder[2], D. Roy[3], S. Hazra[4], S. Mukherjee[5], PP. Sarkar[6*]

[1, 2, 3, 4, 6]Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan, West Bengal, India
[5]Department of AEIE, Murshidabad College of Engineering & Technology, Murshidabad, West Bengal, India

[*]*Corresponding Author: pratim34@gmail.com*

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***Abstract*—** Optics has been recognizing as a good probable signal for realization of logic circuits, digital optical systems for optical communication and computation using optical switching devices for the utilization of super fast speed. Some optical logic gates can operate on the basis of frequency conversion process of some nonlinear materials. Semiconductor optical amplifier is recognized as a very promising and reliable optical device for implementing various all optical logical operations. Recently, more and more advanced technology should be needed to design compact and integrated version of devices. Here the authors have proposed an alternative approach to realize frequency encoded all optical integrated AND - OR logic gate with control input by which a single circuit operates on different logics using reflected semiconductor optical amplifier and add/drop multiplexer type optical switches. Again, this scheme of all optical frequency encoded integrated logic gate using optical switches with controlling input is successfully verified by proper simulation technique.

***Keywords*—**Semiconductor Optical Amplifier, Reflected Semiconductor Optical Amplifier, Add/Drop Multiplexer, Pump Beam, Probe Beam

I. INTRODUCTION

Photon can be used as more suitable information carrier than electron in super-fast information processing, due to its very high speed of operation. For realization of all optical different logical and arithmetical digital devices [1] need different encoding techniques like, frequency [2], intensity, phase, spatial and polarization encodings [3]. Frequency encoding principle is the most reliable technique because frequency of light beam remains unchanged under reflection, refraction, absorption etc. At the time of frequency encoding, two different frequencies of light beams represent two different states of information. Here, presence of light beam of υ_1 frequency is treated as digital logic state '0' and light beam of υ_2 frequency is considered as digital logic state '1'. Now, optical switches like add/drop multiplexer (ADM) [4-7] and reflected semiconductor optical amplifier (RSOA) [8-11] are used to design all optical circuits. Add/drop multiplexer (ADM) is a frequency selecting optical switching device. If ADM is biased by a light beam of particular frequency then the particular frequency of light beam is reflected by ADM if it is coming from input and passes all other frequency of light beam. Opposite incident happens if the biasing is changed. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device, where a weak probe beam with a frequency and a strong pump beam with another frequency are inserted to the input terminals of RSOA. Then this switch will give light beam of frequency of probe beam with power of the pump beam. Therefore RSOA and ADM could be recognized as very useful optical switches for implementing many all optical logical operations.

Here, the authors have proposed a different approach to realize frequency encoded integrated AND-OR logic gate with a control input for selecting particular logic operation with the help of RSOA and ADM. This scheme is successfully implemented on integrated AND-OR logic operations with a single circuit just altering the control input. Also the truth tables have been verified with the simulation result.

The paper is organized as follows, Section I contains the introduction, Section II contains the Scheme of realization of the integrated logic gate, Section III contains the Simulation process of the scheme of integrated logic gate, Section IV contains Results and Discussion and section V mentions conclusions.

II. SCHEME OF REALIZATION OF THE INTEGRATED LOGIC GATE

Here, Two input terminals 'A' and 'B', control input terminal 'C' and one controlled output terminal 'Y' are used to implement the controlling logic unit, which is shown in Figure 1. Now, this scheme of unit provides output as AND as well as OR logic depending upon the control input states of light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies.

A. Scheme acts as AND logic gate

Here, light beam of υ_1 frequency (or digital state '0') is applied to the control input terminal 'C' for realizing this scheme acts as AND logic gate.

1) At first, light beam of υ_1 frequency (or digital state '0') is given to both the input terminals of 'A' and 'B'. So, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 because ADM_1 is biased by υ_2 frequency and this light beam of υ_1 frequency goes as probe beam of $RSOA_2$ and one part of this beam is coming as probe beam of $RSOA_5$. Again, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 as it is biased by υ_2 frequency and one part of this beam goes as probe beam of $RSOA_6$ but other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y' because light beam of υ_1 frequency is present as probe beam of $RSOA_2$. But $RSOA_5$ does not work as there is no pump beam coming from circulator 'C_2'. Similarly, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Again $RSOA_6$ does not have any pump beam coming from circulator 'C_1'. So $RSOA_6$ does not work. Though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3, ADM_3 does not provide any light beam because $RSOA_5$ and $RSOA_6$ do not work. As there is no pump beam of $RSOA_7$ (with constant probe beam of υ_2 frequency) coming from ADM_3, $RSOA_7$ does not work. Actually, some particular RSOA or ADM blocks do not work for respective input combinations. So, only $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y'. It is theoretically satisfied by the first input combination of truth table of AND logic gate, which is given in the Table 1.

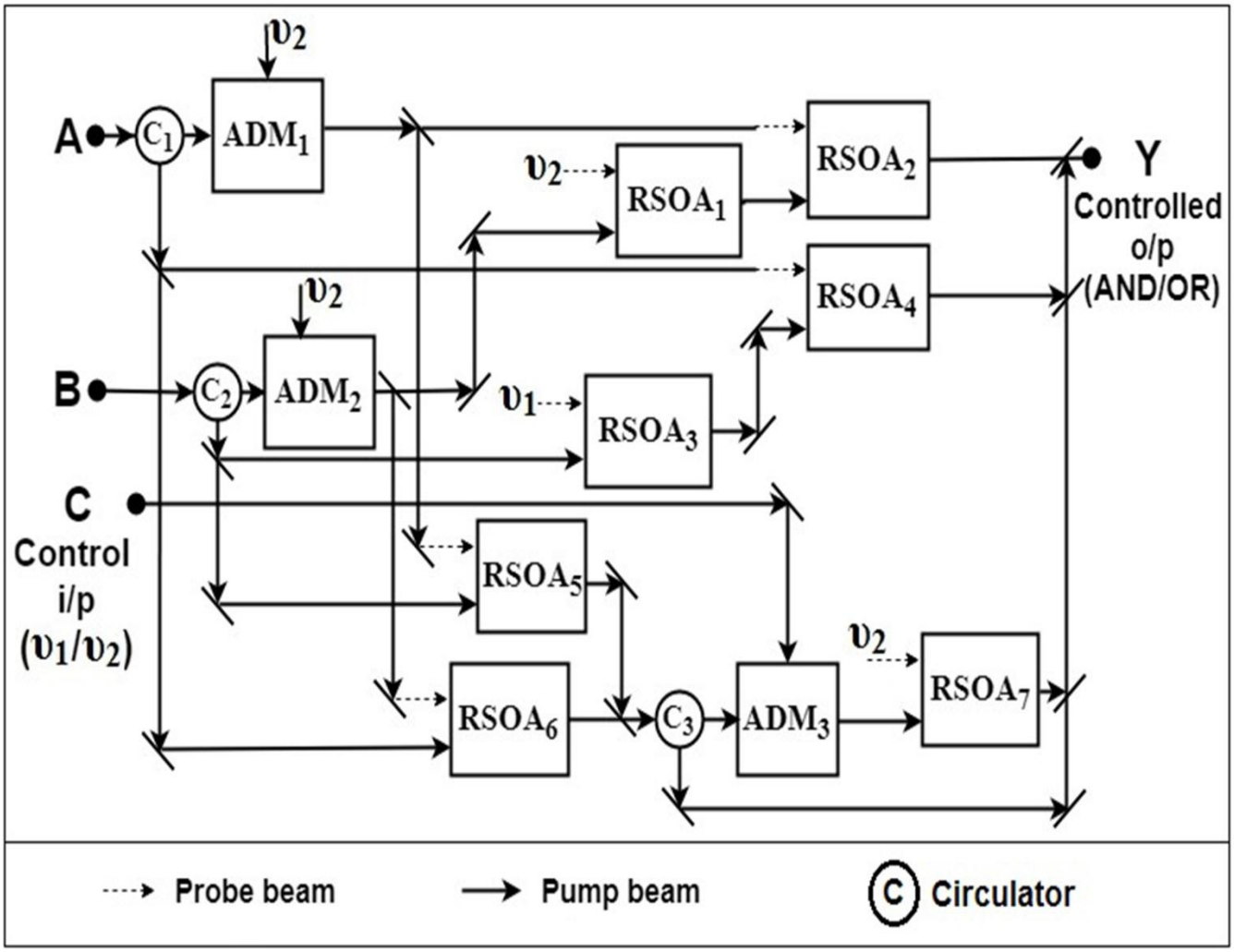

Figure 1. Block diagram of the scheme of integrated logic gate

2) Now, light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies are given to the input channels of 'A' and 'B' respectively. By the similar way, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 and goes as probe beam of $RSOA_2$ and other part of this beam is coming as probe beam of $RSOA_5$. But, light

beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 (biased by υ_2 frequency) and one part of this reflected beam goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. Now, other part of the reflected beam of ADM_2 comes as pump beam of $RSOA_5$. Thus, $RSOA_5$ provides light beam of υ_1 frequency because light beam of υ_1 frequency is present as probe beam of $RSOA_5$. Now, this beam is entering to the ADM_3 which is biased by υ_1 frequency, coming from control input terminal 'C'. So, light beam of υ_1 frequency (or digital state '0') is reflected by ADM_3 and goes to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for absence of sufficient light beams.

3) Here, light beam of υ_2 (or digital state '1') and υ_1 (or digital state '0') frequencies are inserted to the input channels of 'A' and 'B' respectively. Therefore, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 (biased by υ_2 frequency) and this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Now, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 (biased by υ_2 frequency) and one part of this beam goes as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Thus, $RSOA_1$ provides light beam of υ_1 frequency as pump beam of $RSOA_2$. But, other part of the beam, coming from ADM_2, goes as probe beam of $RSOA_6$. Since light beam of υ_2 frequency is present as pump beam, $RSOA_6$ gives light beam of υ_1 frequency to the ADM_3 (biased by υ_1 frequency, coming from control input terminal 'C'). As a result, light beam of υ_1 frequency (or digital state '0') is reflected by ADM_3 and goes to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for lack of proper light beams.

4) Lastly, light beam of υ_2 frequency (or digital state '1') is given to both the input channels of 'A' and 'B' simultaneously. So, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 which is biased by υ_2 frequency and one part of this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Again, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 and one part of the reflected beam comes as pump beam of $RSOA_5$. Whereas other part of this reflected beam goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ provides light beam of υ_1 frequency, which will proceed as pump beam of $RSOA_4$. As a result, $RSOA_4$ provides light beam of υ_2 frequency (or digital state '1') to the controlled output terminal 'Y' because light beam of υ_2 frequency is present as probe beam of $RSOA_4$. Other RSOAs and ADMs do not work due to absence of sufficient light beams though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3.

Table 1. Truth table of the scheme acts as AND logic gate

First input (or Digital form) at channel 'A'	**Second input (or Digital form) at channel 'B'**	**Control input (or Digital form) at terminal 'C'**	**Controlled output terminal 'Y'**
$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$
$\upsilon_1(0)$	$\upsilon_2(1)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_1(0)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_2(1)$		$\upsilon_2(1)$

By this way, after observing the logic output from the controlled output terminal 'Y' for these four input combinations, we can say that, the logic output fully satisfies the truth table of AND logic gate, for control input terminal 'C' as constant light beam of υ_1 frequency (or digital state '0'). This is shown in Table 1.

B. Scheme acts as OR logic gate

For this case, light beam of υ_2 frequency (or digital state '1') is inserted to the control input terminal 'C' for realizing this scheme works as OR logic gate.

1) Here, at first, light beam of υ_1 frequency (or digital state '0') is given to both the input channels of 'A' and 'B' simultaneously. Thus, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 (biased by υ_2 frequency) and goes as probe beam of $RSOA_2$ and another part of this beam is coming as probe beam of $RSOA_5$. Similarly, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 (biased by υ_2 frequency) and one part of this beam goes as probe beam of $RSOA_6$. But other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency. $RSOA_5$ does not work due to absent of pump beam coming from circulator 'C_2'. And $RSOA_6$ is stop for the absence of pump beam coming from circulator 'C_1'. So, there is no light beam for the input of ADM_3 even if light beam of υ_2 frequency coming from control input terminal 'C', which acts as a biasing of ADM_3. Therefore, ADM_3 does not provide any light beam for the pump beam of $RSOA_7$ (with constant light beam of υ_2 frequency). So, $RSOA_7$ does not work. Again, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Therefore, light beam of υ_1 frequency (or digital state '0') from $RSOA_2$ goes to the controlled output terminal 'Y'. It is satisfied by the first input combination of truth table of OR logic gate, which is given in the Table 2.

2) Now, light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies are inserted to the input channels of 'A′ and 'B' respectively. Then, υ_1 frequency, coming from terminal 'A' is passed by ADM_1 and one part goes as probe beam of $RSOA_2$ and other part is coming as probe beam of $RSOA_5$. But, υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 which is biased by υ_2 frequency and one part goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. Now, other part of the reflected beam of

ADM_2 comes as pump beam of $RSOA_5$. Thus, $RSOA_5$ provides υ_1 frequency because υ_1 frequency is present as probe beam of $RSOA_5$. Now, the beam, coming from $RSOA_5$, proceeds to the ADM_3 which is biased by υ_2 frequency, coming from control input terminal 'C'. So, υ_1 frequency is passed by ADM_3 and goes as pump beam of $RSOA_7$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_7$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for absence of sufficient light beams.

3) Next, light beam of υ_2 (or digital state '1') and υ_1 (or digital state '0') frequencies are inserted to the input channels of 'A' and 'B' respectively. Therefore, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 which is biased by υ_2 frequency and one part goes as probe beam of $RSOA_4$ and other part comes as pump beam of $RSOA_6$. Now, υ_1 frequency, coming from terminal 'B' is passed by ADM_2 which is biased by υ_2 frequency and one part of this beam goes as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Thus, $RSOA_1$ provides υ_1 frequency as pump beam of $RSOA_2$. But, other part of the beam, coming from ADM_2, goes as probe beam of $RSOA_6$. Since there is a light beam of υ_2 frequency is present as pump beam, $RSOA_6$ gives υ_1 frequency to the ADM_3 (biased by υ_2 frequency, coming from control input terminal 'C'). As a result, υ_1 frequency (or digital state '0') is passed by ADM_3 and proceeds as pump beam of $RSOA_7$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_7$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y'. Remaining RSOAs and ADMs do not work for lack of proper light beams.

4) Finally, light beam of υ_2 frequency (or digital state '1') is set to both the input channels of 'A' and 'B' simultaneously. Thus, υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 (biased by υ_2 frequency) and one part of this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Again, υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 and one part of the reflected beam comes as pump beam of $RSOA_5$. While another part of this reflected beam goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ provides υ_1 frequency, which will proceed as pump beam of $RSOA_4$. As a result, $RSOA_4$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y' because υ_2 frequency is present as probe beam of $RSOA_4$. Other RSOAs and ADMs do not work for lack of sufficient light beams despite the fact that light beam of υ_2 frequency coming from control input terminal 'C', acts as a biasing of ADM_3.

In this way, the logic output coming from the controlled output terminal 'Y' satisfies the truth table of OR logic gate after analysing four input combinations for control input terminal 'C' as constant light beam of υ_2 frequency (or digital state '1') which is shown in Table 2.

Table 2. Truth table of the scheme acts as OR logic gate

First input (or Digital form) at channel 'A'	Second input (or Digital form) at channel 'B'	Control input (or Digital form) at terminal 'C'	Controlled output terminal 'Y'
$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_2(1)$	$\upsilon_1(0)$
$\upsilon_1(0)$	$\upsilon_2(1)$		$\upsilon_2(1)$
$\upsilon_2(1)$	$\upsilon_1(0)$		$\upsilon_2(1)$
$\upsilon_2(1)$	$\upsilon_2(1)$		$\upsilon_2(1)$

III. SIMULATION PROCESS OF THE SCHEME OF INTEGRATED LOGIC GATE

MATLAB (R2008a) simulink tools have been used for simulation of all optical frequency encoded integrated two input AND-OR logic gate with a control input using optical switches (RSOA and ADM). "I/P 1", "I/P 2", "Control i/p" and " O/P" terminals are used for applying proper inputs and getting proper output. In simulation process, for providing the two frequency states, υ_1 frequency (or, digital state '0') and υ_2 frequency (or, digital state '1') are represented by '3' and '8' respectively. Maintaining the similarity of the block diagram (shown in Figure 1) simulative model of the integrated scheme when acts as AND logic gate is shown in Figure 2 keeping control input as υ_1 frequency or '3'. Another simulative model of the integrated scheme when acts as OR logic gate is also shown in Figure 3 keeping control input as υ_2 frequency or '8'.

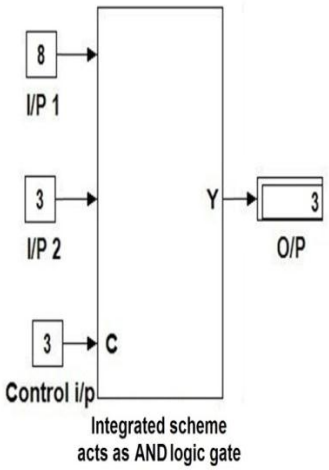

Figure 2. Simulative model of the integrated scheme when acts as AND logic gate

At first, each of the RSOA blocks is properly programmed according to the RSOA mechanism. There are two inputs "pr" for probe beam and "pm" for pump beam and the output "y" in RSOA blocks. According to the theory of RSOA, if we represent pump beam as "3 peta Hz" = υ_1 = digital logic state "0" and probe beam as "8 peta Hz" = υ_2 = digital logic state "1" for understanding the simulation process, then we get "8 peta Hz" at the output terminal of RSOA blocks. The output changes if pump beam and probe beam are altered accordingly.

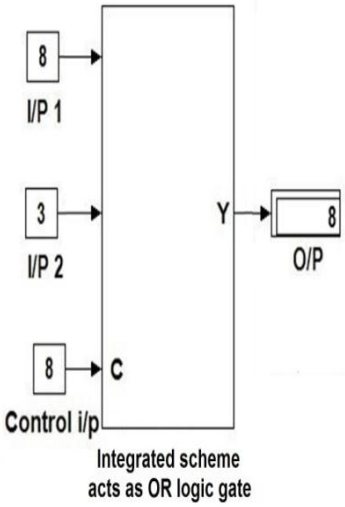

Figure 3. Simulative model of the integrated scheme when acts as OR logic gate

Also, ADM block has been simulated such a way that, it obeys the proper mechanism of ADM. Now, if ADM is biased by a particular light beam frequency, say "3 peta Hz" = υ_1 = digital logic state "0" at "bias" terminal, then this block drops the frequency coming from "input" terminal to "drop" terminal and passes other frequency, say "8 peta Hz" υ_2 = digital logic state "1" to "out" terminal. If the biasing is changed, opposite incident happens.

Finally, RSOA and ADM blocks have been connected in proper way for modelling of the simulative model, which are shown in Figure 4, maintaining the similarity of the theoretical block diagrams in Figure 1.

IV. Results And Discussion

Now, any input combination must be taken into consideration for satisfying the above integrated scheme of all optical digital circuit. If we apply '8' & '3' at "I/P 1" & "I/P 2", and '3' is inserted to "Control i/p" then we can get '3' at the "O/P" (shown in Figure 2). So, this integrated simulative model satisfies truth table of AND logic which is shown in Table 1. But, when '8' is inserted to "Control i/p" then we can get '8' at the "O/P" (shown in Figure 3). Therefore, we can say that, this integrated model satisfies truth table of OR logic which is shown in Table 2. This integrated simulative model can also be satisfied by the other input combinations of the truth tables of respective AND and OR logic gates.

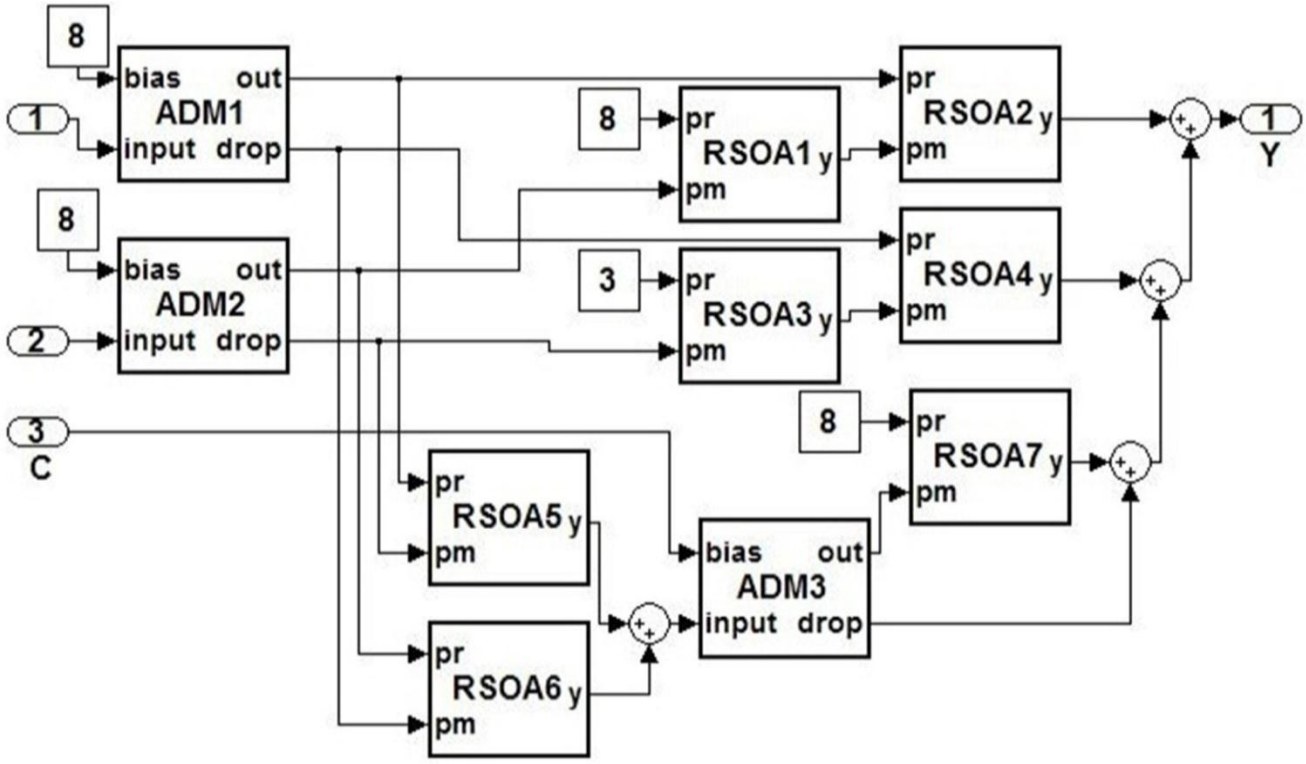

Figure 4. Internal simulative model of the integrated scheme

V. Conclusions

The simulative verification satisfies this integrated AND-OR logic gate with control input. For that reason its functionality can be utilized directly or indirectly for developing and verifying the performances of other optical frequency encoded digital arithmetic and logic circuits. Also, one can implement various schemes of all optical integrated logic and arithmetic circuits using this technique for optical computation. With the advancement of circuit integration complexity, it may be easy to construct advanced optical computer by combining several all optical digital devices or circuits in near future. The control input provides the opportunity for selecting particular logic operation of the integrated scheme of all optical logic circuits.

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Authors Profile

Mr. B Ghosh pursed Bachelor of Engineering from University Institute of Technology, University of Burdwan, Burdwan in 2011 and Master of Engineering from University of Burdwan in 2014. He is currently pursuing Ph.D. and working as Part–time Guest Lecturer in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, since 2014. He has published around 10 research papers in peer-reviewed journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. His main research work focuses on Optical computation, Semiconductor optical amplfier and photonics. He has 5 years of teaching experience and 3 years of Research Experiences.

Mr. N Halder pursed Master of Engineering from IIT, Kharagpur in year 2011. He is currently pursuing Ph.D. also working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2012. He has published around 10 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and international conferences. His main research work focuses on Image Processing and Sensors. He has 6 years of teaching experience and 4 years of Research Experiences.

Dr. D Roy pursed Ph.D. from IIT, Kharagpur and currently working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2012. He has published around 20 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. His main research work focuses on Nanoelectronics and Microelectronics. He has 6 years of teaching experience and 6 years of Research Experiences.

Mr. S Hazra pursed Master of Technology from University of Burdwan in 1999. She is currently pursuing Ph.D. and working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan since 2002. She has published around 5 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and international conferences. Her main research work focuses on Semiconductor optical amplfier and photonics. She has 19 years of teaching experiences.

Mr. S Mukherjee pursed Master of Technology. He is currently pursuing Ph.D. and working as Assistant Professor & HOD in Department of Applied Electronics and Instrumentation Engineering, Murshidabad College of Engineering & Technology, Murshidabad. His main research work focuses on Optical computation, Semiconductor optical amplfier and photonics. He has 8 years of teaching experience and 2 years of Research Experiences.

Dr. PP Sarkar pursed Ph.D from Jadavpur University. He has been currently working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2008. He has published around 15 research papers in peer-reviewed international journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. He is also a reviewer of different reputed Journals & Conferences. His main research work focuses on Parrallel computing, optics and photonics. He has 17 years of teaching experience and 10 years of Research Experiences.

