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A Survey on Performance Optimization of Cache Memory in the Individual Nodes of Wireless Sensor Networks

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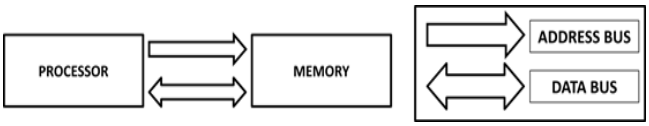
***Abstract*—** The wireless networks are constrained networks with limited battery backup and memory. The nodes in the Wireless Sensor Network use memory buffers to keep track of the sequence number of the Transport layer segments. This helps to resend the packets during the time of packet loss. The fast retransmission of the lost packets is done by nodes of Wireless Sensor Network with the help of fastest form of memory called as cache memory. This helps to achieve reliability. Understanding the working of cache memory in fulfilling such a great responsibility is a challenge. The survey has been conducted to understand the different types of processors and memories that could be used in the nodes of wireless sensor networks. An overview of optimization methods on cache memory and cache mapping mechanisms to improve the performance of the cache are also studied.

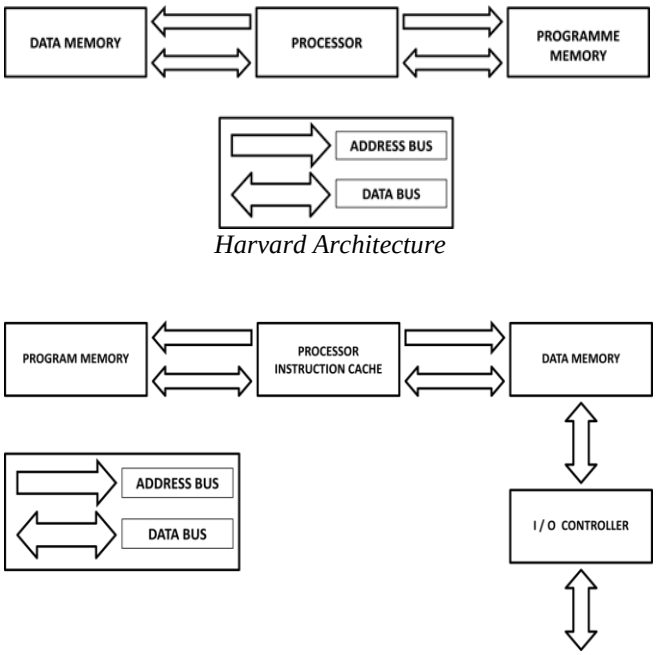
Keywords— *Wireless Sensor Networks (WSN), Cache memory, performance optimization, survey*

I. INTRODUCTION

The wireless networks are constrained networks with limited battery backup and memory. They have the advantages of connecting multiple devices to the same internet connection. They allow mobility of different mobile devices like laptops, mobile phones and tablets to move around in the network area spontaneously and still maintain the connection to the internet. Unfortunately, these networks suffer high chance of packet loss not only due of lossy channels but also due to congestion in the underlying network. To address such an issue, researchers make use of reconfigurable cache at the intermediate nodes. The Nodes of sensor network can be designed using Von Neumann architecture, Harvard architecture or Super Harvard architecture. Figure 1 shows the architecture of the wireless sensor network nodes. Each node in a Wireless Sensor Networks has a Controller, Communication devices, Sensors or actuators, power supply and memory [1,4]. The Figure 2 shows the structure of a wireless sensor node.



Von Neumann Architecture



Harvard Architecture

Super Harvard Architecture

Figure 1. Architectures of Wireless Sensor Network Nodes

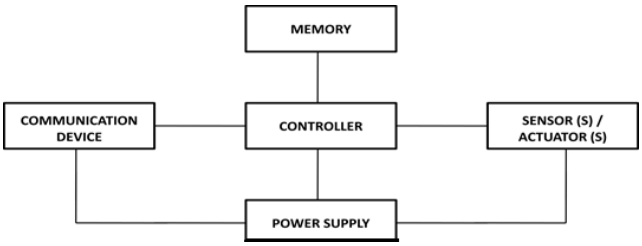


Figure 2. Structure of Wireless Sensor Network Nodes

The cache memory in sensor nodes helps in speeding up the period of time between the Random-Access Memory and the CPU. Pre-fetching of the required data from the main memory for the processor, prior to the processor requests is achieved using cache memory. The locality of reference [2] is the main principal behind data pre-fetching.

The major constraints during the design of any cache memory are the performance, power consumption and the area available as a cache. With these constraints in mind, the cache researchers came up with the three cache organizations called direct mapped cache, associative cache and set associative cache [3]. This survey is proposing to adopt the best possible mapping technique for a sensor node.

II. RELATED WORK

Multiple works have been deployed to increase the performance of the WSNs [5][6]. Some work mainly concentrates on the protocols which utilizes the cache memory to avoid congestion. One such work is implementing the Distributed Transport protocol for Sensor Networks (DTSN). The DTSN is implemented with fixed transmission window and without congestion control mechanism for testing the congestion. The works conclude that the optimum usage of cache is achieved during congestion avoidance.

Adam Dunkels, etal [7] proposed different Mechanisms like Distributed TCP Caching (DTC) for WSNs that have been deployed to increase the reliability of the network. Segment caching and local retransmission using cache are the major ideas in DTC to sidestep end to end retransmissions. This work helps to reduce power consumption by TCP sender & receiver nodes and increase the throughput of the network by caching the segment with highest sequence number at the nodes closer to the receiver. The work Guarantee the throughput of network but not the cache.

Works on protocols like End-to-end Reliable and Congestion aware Transport layer Protocol (ERCTP) [8] for heterogeneous WSNs are surveyed in this work. The protocol developed is divided in to two modules namely congestion control module and Reliable module. The congestion control module is further divided in to congestion detection module, congestion notification module, rate adjustment modules. This paper concludes that, by introducing distributed memory caching, helps to aware the congestion by congestion aware module, and reliability by reliable module. Performance optimization techniques for optimization of WSNs such as Cross-layer caching [8] were implemented to understand the transport layer NACK repair and MAC layer adaptive retransmission processes to achieve reliability. The work also concludes that NACK and adaptive retransmission enriches the advantage of intermediate caching. Works related to reducing the overall energy ingesting and the file transfer extent were conducted by improving DTCP Caching for WSNs [9]. Each node will cache the TCP segments. The acknowledged segments are unlocked, and unacknowledged segments are locked. This helps in retransmission and in turn helps in reliability. The author states, that these types of works help in understanding TCP window size and TCP caching performance.

Different surveys of transport protocol for WSNs [10] have been conducted to help to understand the different transport protocols that can be used in WSN. But, the study discusses only about the retransmissions of the lost data during transmission but not specifies how it is to be retransmitted. The study also does not mention the use of cache memory in the nodes.

Protocols like Reliable Multi-Segment Transport (RMST) [11] were introduced to propose a diffusion architecture where the sink subscribes to the interest. The interest will then publish the type of data it is interested in the form of attribute & value pairs. All other nodes having the data will revert. Cache is used in 2 modes, the mode of caching and a mode of non-caching. In mode of caching, one major node maintains a cache locally & all other nodes make use of the major cache. In mode of non-caching every sources and sinks sustain their own cache. Cache entries have fragment map (actual data) & hole map (timer). The work fails to specify which cache mapping techniques to be used to achieve maximum usage of both cache modes in order to achieve reliability.

Pump- slowly, fetch quickly (PSFQ) [12] is a Reliable transport protocol for sensor networks, that was introduced to help data distribution from source at very slow rate and collection of lost data from the neighbouring nodes at highly aggressive rates. The pump function of PSFQ likely performs controlled flooding and needs every transitional node to have a data cache to be used during local loss recovery and during the time of in-sequence data delivery. To improve the reliability of a WSN Multi-path-based Distributed TCP Caching (MDTC) [13] was introduced. MDTC implemented path redundancy and local retransmission. When each node receives the data, it caches the data and sets timer for the incoming data. The nodes wait for the ACK of the packet. If the ACK is not received in the incoming data timer, node's

cache is locked and timer for retransmission is started. When the timer for retransmission elapses, the cached packet in the nodes are used for retransmission and the transmission timer is set again.

Works on cache coherence within the networks [14] were implemented to study the read and write requests of each node in the network. The work does not specify which cache mapping techniques to be used during read and writing in to the cache.

Different MAC protocols for energy efficient Wireless Sensor Networks [15] were developed to make the network energy efficient by involving the nodes in periodic listen and sleep modes to reduce the energy consumption. But, the work fails to specify the contribution of cache memory in saving energy during retransmissions of lost or corrupted data.

In all the literatures cited above, most of the authors did not specify which cache mapping and optimization techniques to be used during reading and writing of data in to the cache.

III. METHODOLOGY

To optimize the performance of cache memory in the nodes of wireless sensor networks, the following points are to be considered.

- Miss rate reduction
- Miss penalty reduction
- Reduction in the time to hit in the cache

A. Miss Rate Reduction

While attempting to access data from the cache, if the process is unsuccessful, main memory access is required to retrieve the data and long latency in cache access is encountered. This phenomenon is known as cache miss. The survey studies the three different types of cache misses [16] known as Compulsory miss which is also known as Cold miss, Conflict miss and Capacity miss. The Cache misses encountered during the first-time access are called as compulsory misses.
Conflict miss is a cache miss that occur when we require a data that was available in the cache some time back but erased from the cache currently. Conflict miss can be measured by considering the difference between the numbers of miss of two cache memories with same cache size and block size, but one with limited and other with full associativity. The Capacity miss is a cache miss that occurs because of the availability of less size in the cache memory irrespective of their mapping techniques. Capacity misses are the cache misses that are very difficult to identify and rectify. The cache misses that still appear after taking the difference between compulsory and conflict misses are called as capacity misses.

B. Miss penalty Reduction

The average memory access time of a processor decides the performance of a processor and can be given as in equation (1),

$$AT=HT+MR*MP \quad (1)$$

Where, AT is the average access time, HT is a Hit time which can be defined as the time required to deliver a block of data from cache to processor, MR is Miss rate and can be defined as the cache misses per cache references and MP is the miss penalty which can be defined as additional time that is required for a processor due to cache miss. Miss penalty directly affects the average access time.

C. Reduction in the time to hit in the cache

The data requested are not available in the cache until address translations are performed. Hence, there is need to avoid address translations while indexing the cache in order to reduce hit time. For this purpose, set index are taken from the page offset portion of the virtual address.
Address translation can also be avoided by indexing the cache directly by virtual address.

To reduce the cache miss rates, different optimization methods or techniques are used. The compulsory misses are reduced by the Data prefetching technique. Data prefetching helps the microprocessor to request for the data whose computation is not already started. Prefetching instructions can either be hardware or a software. An example of hardware prefetching is Sequential prefetching.

Prefetching of the data by cache memory will be successful if the data is predicted. Data prediction can be done either by hardware or by the software instruction specially designed for data prefetching. Data prefetching will also be successful when there exists enough space in the cache memory to handle the previously retrieved data and the previously fetched data that are active.

Compulsory misses are condensed by snowballing the block size of the cache to certain extent to maintain spatial locality. To certain extent, increasing the associativity can reduce the conflict miss. The conflict miss can also be reduced by changing the size of the arrays used as data, changing the starting address of the variables, array transpositions and combining multiple arrays. Array padding [18, 10 and 20], Intra array padding, array merging or group and transpose [21], Data copying are some of the techniques to reduce the conflict miss. All of these techniques are termed as Optimization of data layouts, which helps not only in reducing the conflict miss but also the false sharing [17].
Capacity miss can be reduced by using loop blocking or loop tiling techniques. [22, 23, 24].
To reduce the miss penalty there are four following techniques,

- Multi-level Caches

- Critical word first and early restart
- Properties to read misses over write misses
- Victim caches

A. Multi Level Caches

Multilevel caching is a technique used to avoid miss penalty by introducing another level of cache between the actual cache and the main memory. The technique requires extra hardware support.

B. Critical word first and early Restart

Critical word first technique first requests for the word that was missed in the cache and sends it to CPU as soon as it is available. The technique is also called as wrapped fetch. The technique is impatient since it does not allow complete word to be loaded.

Early restart helps to fetch the data in the normal order but when the requested data is fetched it sends the data with highest priority to the processor.

C. Properties to read misses over write misses

Read misses are the cache misses that occur when an attempt is made to read the data from the cache before it was written in to the cache. To avoid read misses a write-through cache with write buffer of enough size can be used.

D. Vicctim Caches

The victim cache technique uses fully associative cache memory of a tiny size to remember the data that was discarded previously. The idea behind the approach is that the data discarded may be needed in the near future.

IV. OBJECTIVE AND DISCUSSION

The critical factor of a node in the WSN is its cache memory. The cache is designed to overcome the speed gap during instruction execution and hence it is important to study the performance measurement and metrics of cache memory during the design of the WSN nodes.

The cache misses and the cache hits play a vital role in determining the performance of the cache memory. The cache misses and hits help to determine the Average Access Time, which is one of the most important performances metric.

Other than Average Access Time, performance of the cache also depends on cache size and cache mapping techniques. Hence in the proposed survey following objectives have been considered.

- To propose best suited cache mapping and optimization mechanisms to reduce conflict misses and miss penalties in the nodes of WSN.
- To propose an optimal size for a cache memory to reduce capacity misses, a factor of miss rate in the nodes of WSN
- To propose energy efficient and reliable cache performance WSN.

V. CONCLUSION AND FUTURE SCOPE

The wireless networks are constrained networks with limited battery backup and memory. The nodes in the WSN use memory buffers to keep track of the sequence number of the Transport layer segments. This helps to resend the packets during the time of packet loss. The fast retransmission of the lost packets is done by nodes of WSN with the help of fastest form of memory called as cache memory. This helps to achieve reliability. Understanding the working of cache memory in fulfilling such a great responsibility is a challenge. The structure of wireless sensor node consists of a Controller, Communication devices, Sensors or actuators, power supply and memory. The controllers that can be used in the wireless sensor nodes can be Texas Instruments MSP430 and Atmel ATMega 128L. Texas Instruments MSP430 is a 16-bit, RISC core processor with the clock cycle of up to 4 MHz and available in different versions with 2-10 kb RAM. Texas Instruments MSP430 is provided with several DACs and the price starts at 0.49 US$. Atmel ATMega 128L is a 8-bit controller, with larger memory than MSP430 but, it is slower than MSP430.

The MSP430F15x/16x/161x are microcontroller configurations that has dual 12-bit Digital to Analog converter, dual in-built 16-bit timers, a high speed 12-bit Analog to Digital converter, at most two universal serial synchronous or asynchronous communication interfaces (USART), I2C, 48 Input or Output pins and Direct memory access (DMA). The process in which the sub system of hardware of a computing device gets access to the random-access memory without the intervention of central processing unit (CPU) is known as Direct Memory Access. MSP430 series provides extended addressing of Random-Access Memory for applications which are memory-intensive and applications with the requirements of large C-stack.

It is observed from the survey, that most of the WSN nodes use the controllers of Atmel family. There are two spaces of main memories in Atmel Atmega 128L, the data and the program memory spaces. It also consists of EEPROM used for data storage, contains in system on-chip flash memory of 128kb and reprogrammable for program storage. The flash program memory is further divided in to two parts and are called as Boot program section and application program section. Atmega 128L also contains a SRAM which acts as a cache memory and has a size of 4kb.

Understanding the working of SRAM of Atmega 128L as a cache memory and improving the performance of SRAM as a cache in order to improve the reliability is a challenge. Summarizing the above paragraph, the main problems involved in improvising the performance of WSN are,

- To determine most favorable cache size to account for the cache hits / misses to optimize the performance.
- To adopt best mapping and optimizing techniques to read and write the data into cache for better results in performance of the cache and entire network.
- To analyze network reliability and energy efficiency based on the impact of change in cache size and mapping technique.

The Power law of cache misses helps to test the performance of the cache memory by increasing the size of the cache memory and testing the number of cache miss. This testing technique requires having a reference of number of cache miss of any one particular cache size. Hence, in the further research the output of Atmel Atmega 128L microcontroller will be taken as the reference cache miss.

The performance of the cache can also be tested using a technique called as Stack distance profiling, in which cache miss is measured by implementing the different associativity or the cache mapping techniques on the cache. The proposed work uses this technique to Compare different cache mapping techniques currently in use and obtain the best cache mapping technique for enhancing the performance of WSN. With the results of testing the performance of the cache of WSN node, the best cache size and mapping technique of the cache is determined and can be tested on different protocols like, DTCP, ERTCP, RMST, PSFQ and MTDC which could help in increasing the reliability of the WSN.

In this survey an effort is made to investigate the performance of the WSN by understanding the different types of cache mapping techniques on the cache memory of different size of an individual node in a WSN. The work also helps to adopt the best suited mapping mechanisms and optimal size for the cache memory of the nodes to reduce conflict misses and capacity misses in the cache. The work helps to optimize the performance of the cache and also the entire WSN. Increasing the performance of cache memory in the individual nodes of WSNs will in turn decrease the delay in resending the lost packets in the WSN. Thus, the performance of the entire WSN is increased.

Proposed work helps in increase the speed of packet retransmission by optimizing the performance of the cache and thus we can increase the reliability of the network. This work can also help to save energy - The most important resource of the WSNs.

Wireless sensor networks are the constrained networks with limited resources like battery and memory. Multiple works have been deployed in order to save energy and increase the performance of the WSN in terms of reliability, security and scalability.

Proposed work has surveyed different literatures used to increase the performance of the WSN. Most of the researchers propose different protocols that increase the reliability of the network by caching the data in the cached memory and using the cached data for retransmission during the situation of congestion.

However most of these researches does not show the structure, implementation, size and mapping mechanisms of the cache memory used to store the data used for retransmission.

The survey and hence the future work help in understanding the structure, implementation, size, mapping mechanisms and different optimization techniques of the cache memory used to store the data which is used for retransmission and thus helps to optimize the performance of individual nodes in the WSNs in terms of reliability and energy efficiency.

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