

# Minimizing Energy Consumption in The Multicore Processors Using Energy Aware Variable Neighborhood Search

Prabhjot Kaur<sup>1\*</sup>, Manoj Agnihotri<sup>2</sup>

<sup>1,2</sup>Department of Computer Science & Engineering,  
Amritsar College of Engineering and Technology, Manawala, India

Available online at: [www.ijcseonline.org](http://www.ijcseonline.org)

Received: 22/Jun/2016

Revised: 10/Jul/2016

Accepted: 16/Aug/2016

Published: 31/Aug/2016

**Abstract:** - Energy consumption is found to be critical task in today’s high performance computing. Consuming the energy in efficient way is still an open area of research. This paper has proved that the use of heuristics like Greedy method, Random method etc doesn’t provide consistent result every time when scheduling process is being run. Greedy can’t guarantee global optimal solution however Random method based upon certain global ability sometime may get best solution sometime may not. The use of variable neighbourhood search algorithm ignore in resistant task allocation for multicore processor. So in order to overcome these issues a variable neighbourhood search based approach is proposed to decrease the energy consumption rate.

**Keywords**— Green computing, energy consumption, variable neighborhood search

## I. INTRODUCTION

Green Computing is the environmentally capable and eco friendly benefit of computers and their devices. “Greening” your processing equipment may be a low-risk strategy for your company to not just help the environmental surroundings but also scale back costs. Additionally it is one of the main rising trends running a business nowadays. Building an aware choice to move inexperienced in the workplace, not just increases your bottom line, but also reduces your carbon footprint. It is a win-win irrespective of however you look at it. Green Computing or Green IT describes environmentally home processing or IT. it’s “the analysis and notice of planning, making, using, and eliminating pcs, servers, and related subsystems—such as for example watches, units, storage products, and marketing and communications Systems—successfully and efficiently with minimal or number affect the surroundings.

Green IT also works to attain economic viability and increased system performance and use, while abiding by our social and ethical responsibilities. Hence, Green IT involves the measurements of environmental sustainability, the economics of power performance, and the sum full cost of possession, which include the price of disposal and recycling. It is the research and practice of using processing methods efficiently.

Green research practices range from the implementation of energy-efficient major handling goods (CPUs), machines and peripherals as well as repaid resource use and right treatment of digital invest (e-waste). Contemporary IT practices depend upon an intricate mix of individuals, systems and electronics; consequently, all natural research

energy should undoubtedly be endemic in character, and manage significantly revolutionary problems. The Power Celebrity manufacturer turned a principal considerable, definitely in notebook pcs and displays. Like applications have today been picked in Europe and Asia. Green processing methods arrived to real in 1992, even though Environmental Protection Firm (EPA) launched the Power Star program. Green processing can be referred to as green information technology (green IT).



Figure1. Green Computing

### ADVANTAGES:-

- Conserving sources suggests decrease energy is required to produce, use, and get rid of services and products
- Preserving energy and sources preserves money.

- Natural processing actually contains adjusting government policy to encourage recycling and lowering energy use by persons and businesses.

#### DISADVANTAGES:-

- Natural processing could actually be quite costly.
- Some computers which can be natural may be significantly underpowered.
- Rapid engineering change

**Energy Aware Scheduling:-**In power-aware scheduling [16], jobs are scheduled to nodes in such a method to reduce the server's overall power. The largest operating cost sustained in a Cloud data center is in operating the servers.

**Thermal Aware Scheduling:-**In thermal-aware scheduling [17], jobs are scheduled in such a way that reduce the entire data center temperature. The target is not always to conserve the energy used to the servers, but instead to reduce the energy needed to operate the data center cooling systems.

#### A. Introduction of multicore processor

A multi-core processor is an integrated world (IC) to which two or more processor has now been attached for improved performance, paid off power usage, and more efficient parallel running of multiple tasks. With the increment in count of research cores per processor, which means requisite for flexible research schemas that may brutalize the simultaneous performance of the recommendations and may accommodate adequate recurrence at the same time and trading data process also increases. Early in the day parallel handling schemas are built sometimes on meaning passing standards (like MPI) or on frequent storage schemas (like OpenMP framework). It is simple to program and debug in OpenMP like framework than MPI since OpenMP is based upon provided storage schemas and also the rule maintenance of OpenMP is simpler than MPI.

The Chart Minimize framework is extensively utilized in different distributed structures like information centres for the adequate and computerized research, planning and allotment of jobs to numerous model hubs. The similar idea can be owned for the coding of adjustable primary frameworks as on account of the Phoenix Chart Minimize schema that is expected in the information centre Chart Minimize functions. Nevertheless, the whole performance of the multi-core frameworks is decreased by the overhead of work scheduling utilizing the Chart Minimize framework. The necessity for factory stage data centres who hosts a big amount of models has been caused for providing web purposes such as for example packing movie, sites and cloud handling. In this adjustable centered diagram twin primary processor chips is shown in wherever two

processors are fixed employing their local storage, one system bus and one system closet and each processor chip is split into two Cores.

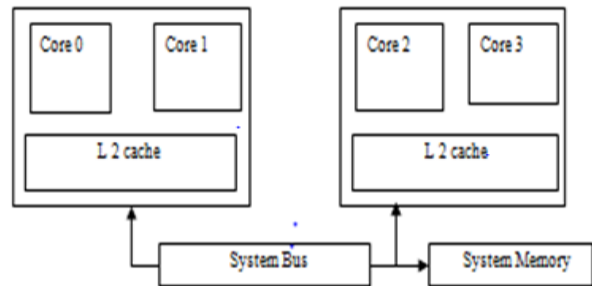


Figure2. Multicore processor architecture

#### B. Performance, Energy and temperature optimized scheduling

The running multicore architecture is now integrated part of wide selection of research process ranging from powerful to standard function research and embedded to portable system. The amount of cores in a system can vary everywhere from handful of cores to thousand of cores. The upsurge in computational efficiency reached with the addition of more cores to chip present energy and thermal issues. Provided job collection, energy and thermal aware scheduler needs to choose the duty key mapping as well as the order and frequency of execution of every job to guarantee the preferred energy and thermal answer of the system. Choice room expansion with improve amount of cores and get a handle on variable (number of frequency level, sleep states) present another barrier to planning minimal cost efficient scheduling schemes.

This paper is organized as follows. At first, Section 1 contains the introduction of the green computing and multicore processor. Section 2 focus literature reviews on techniques used in multicore processors. Section 3 introduces the problem formulation which we can find in existing work. Section 4 describes the technique which is used in the proposed work and their model and explains the methodology with flow Chart. At the end, the finding is concludes research work with future direction by improving the values of parameters.

## II. LITERATURE SURVEY

Yi Xiang et.al Soft and Hard Reliability-Aware Scheduling for Multicore Embedded Systems with Energy Harvesting (2015) [2]

Energy harvesting driven for multicore stuck system, it is vital to create intelligent source allocation techniques that adjust the applying performance methods on the travel to change the harvesting system to adjusting energy supply. Author presented a cross design-time/run-time frame of

guide for source allocation that requires in focusing variations in solar radiance and performance time, variable problems, and lasting problems due to aging impacts. Empirical results established that platform shown improvements in efficiency and adaptively.

Santanu Sarma et.al Cross-Layer Exploration of Heterogeneous Multicore Processor Configuration (2015) [3].

Heterogeneous multicore processors (HMP) directed at implicit benefits over homogenous multiprocessors due to their increased energy, performance, and energy effectiveness for certain chip/die area. For the reason that report, we directed at a cross-layer strategy for discovering and establishing a HMP for certain process goal below process stage restrictions (such as equal area or energy budget) as an optimization complication.

Connor Imes et.al POET: a portable approach to minimizing energy under soft real-time constraints (2015) [6].

Embedded real-time programs must meet timing restrictions while reducing energy consumption. These alternatives aren't communicable, but, and when the applying or the software improvements, these solutions should be redesigned. That report addressed the problem of concern and exploiting normal tradeoffs, applying get a handle on idea and mathematical optimization to reach energy minimization. Publishing lightweight, energy-efficient concept for embedded system.

Benjamin Betting et.al Evaluation and Superiority Analysis of Decentralized Task Control Mechanism for Dependable real time SOC Architectures (2013) [5].

This short article showed the concept of an artificial hormone system for recognizing a fundamentally decentralized home arranging and real-time variable task control device applying self-X properties. Evaluation and superiority analysis of a AHS managed SOC towards other techniques in centralized or partially decentralized way like feedback controllers and complicated multi-agent. Furthermore, in article validated and compared the expense for size, transmission and computation with regards to the development in system reliability.

Hafiz Fahad Sheikh et.al Simultaneous optimization of performance, energy and temperature for DAG scheduling in multicore processors. (2012) [7].

This report addressed the combined optimization of performance, energy, and temperature, termed as PET - optimization. That multi-objective PET-optimization was achieved in scheduling DAGs on multi-core systems. That method has been based on multi-objective evolutionary algorithm (MOEA) for finding Pareto optimal alternatives using scheduling and voltage selection. The proposed algorithm acquired the Pareto vectors (or fronts) efficiently.

The potency of the proposed algorithm is that it achieves diverse range of energy and thermal improvements.

H.F.Sheikh et.al Fast algorithms for thermal constrained performance optimization in DAG scheduling on multi-core processors (2011) [8].

Thermal administration has been extremely vital for successful exploitation of enormous computational energy made available from advanced multi-core processors. Without the thermal constraint, a job graph might be scheduled at their maximum voltage. In that report Author has been presented two formulas for reducing the efficiency deterioration and the similar overhead. The proposed formulas, named PAVD, and TAVD. TAVD selects the tasks which gained maximum heat while PAVD selects the tasks with the minimum efficiency penalty.

### III. PROBLEM FORMULATION

While optimizing performance we may focus on overall Delivery time, throughput, and Produce span. Because of the reality, that work centers around the arrangement of DAGs and picked routine length for development in performance. It can decrease the escalation in routine length resulting as a result of changes needed to satisfy the thermal constraints. With an emphasis on power and thermal dilemmas, the natural computational rate of the processors can just only be harnessed with powerful arrangement and mapping tools. High energy consumption also can cause unacceptably high conditions that subsequently may result in the loss in performance, stability and lifespan, and also overall failures.

Many multi-core chips are now designed with systems to control their power. Software-based systems for dynamic power and thermal management (DPM and DTM) may be made to use reduced level control characteristics such as for example frequency climbing, time gating, and rest states to boost the power consumption and thermal profile of the system.

The utilization of heuristics like Greedy technique, Random technique etc does not give regular effect everytime when arrangement method has been run. Greedy can't promise worldwide optimum alternative however Random technique in relation to particular worldwide ability sometime may get best solution sometime may not. The utilization of variable neighborhood search algorithm ignore in resistant job allocation for multicore processor. The graph showing dependence of system power consumption on the CPU clock frequency under maximum load is of quite typical shape:

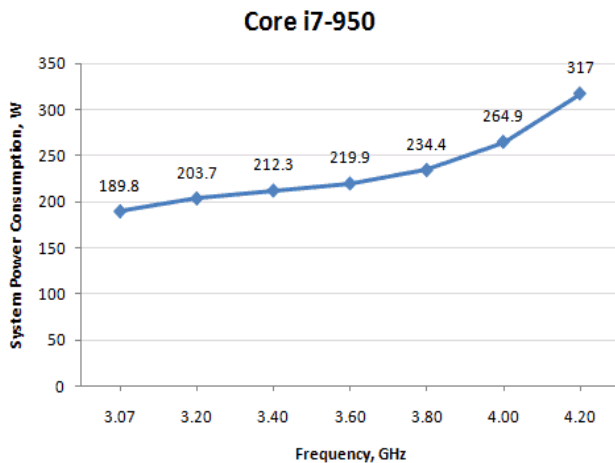


Figure3. Power consumption curve of an Intel Core i7 950 CPU diagram [18]

IV. TECHNIQUE

Systematic change of neighborhood within a possibly randomized local search algorithm produces a easy and efficient metaheuristics for combinational and global optimization called variable neighborhood search. Thus as well as providing very good alternatives, often in easier methods than other techniques, VNS gives insight into the reasons for such a performance, which often lead to more efficient and innovative implementations. Despite their ease it shows to be effective. Variable community research technique is on the basis of the following central observations:-

- A nearby minimum w.r.t. one community structure is certainly not domestically little w.r.t. still another community structure
- A global minimum is domestically optimal w.r.t. all community structures
- For several problems, local minima regarding one or several neighbourhoods are somewhat close to each other.

Variable community research (VNS) is really a metaheuristics, or a construction for creating heuristics, based on systematic improvements of neighbourhoods equally in ancestry stage, to locate a local minimum, and in perturbation stage to emerge from the equivalent valley. It was initially planned in 1997 and has since then fast developed equally in their strategies and their applications.

Moreover, one part is devoted to newcomers. It consists of measures for creating a heuristic for any unique problem. Those measures are typical to the implementation of different metaheuristics.

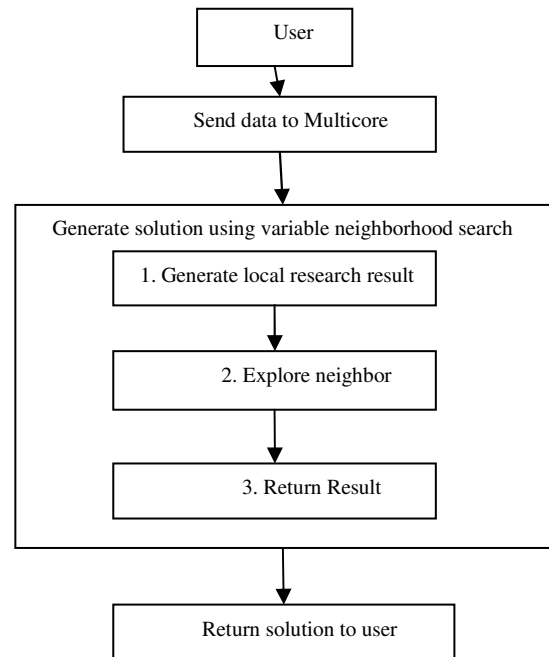


Figure4. Block diagram

In block diagram, user can send the data to multicore processor and Generate solution using variable neighborhood search then generate local research result and explore the neighbors and return the result and then return solution to the user.

Flow chart:-

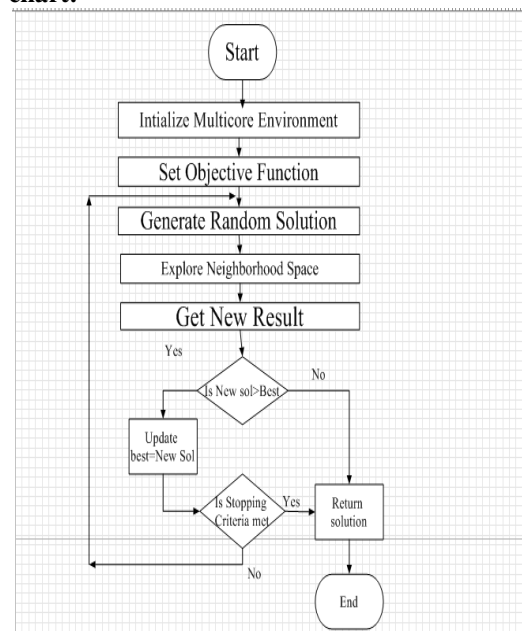


Figure5. Proposed Approach

In proposed Approach, we explore a new technique variable neighborhood search for generating random

solution and getting new result. If new solution is greater than best then update new solution is equal to best and after criteria met with best then return solution otherwise again generate random solution.

**Step I:** Start and Initialize multicore environment

**Step II:** After initialize, set the objective function in multicore environment.

**Step III:** Generate the random solutions for different parameters.

**Step IV:** Explore the neighbor space for random solutions.

**Step V:** after exploring neighbor space get the new result.

**Step VI:** If new solution is greater than best then update best=new result and if stopping criteria met then return solution and end the process. if stopping criteria is not met then generate random solution again.

**Step VII:** If new solution is not greater than best then return result and end the process.

### CONCLUSION AND FUTURE WORK

Greedy cannot assure global optimal solution but Random method based on specific global ability sometime may get best solution sometime may not [1]. The use of variable neighborhood search algorithm ignores in tolerant task allocation for multicore processor. So in order to overcome these issues a variable neighborhood search based approach is proposed to decrease the energy consumption rate. A comparison using heuristic approaches with variable neighborhood search by considering certain parameters will be performed. The parameters are:-Performance, Energy, Temperature, Make span Time, Speed up.

### ACKNOWLEDGMENT

This research was supported by Amritsar College of Engineering And Technology, Manawala. We are thankful to our colleagues who provided expertise that greatly assisted the research, even though they do not take credit with all of the interpretations provided in this paper.

### REFERENCES

- [1] Sheikh.H.F. And Ahmad.I, "Efficient Heuristics for Joint Optimization of Performance, Energy, and Temperature in Allocating Tasks to Multi-core Processors," International Green Computing Conference (IGCC), pp.1-8, Nov 2014.
- [2] Xing Yi, Pasricha sudeep, "Soft and Hard Reliability aware scheduling for multicore embedded System with energy harvesting" IEEE Transaction on multiscale computing System, vol. 1, pp no. 220-235, Dec 2015.
- [3] Sarma Santanu, Dutt Nikil, "Cross Layer Exploration of heterogeneous Multicore Processor Configuration" 28<sup>th</sup>

- International Conference on VLSI Design , pp. 147-152, 2015.
- [4] Cuesta David, Acquaviva Andrea, Ayala Jose'L, Hidalgo jose'I, Atienza David, Macii Enrico, "Adaptive Task Migration Policies for Thermal Control in MPSOC's" ,VLSI 2010 Annual Symposium, pp-110-115, 2010.
- [5] Betting.B, Brinkschulte.U, Pacher.M, "Evaluation and Superiority Analysis of a decentralized task control mechanism for dependable real time SOC Architectures," 16<sup>th</sup> IEEE International symposium on object/component/service oriented Real time distributed computing (ISORC), pp. 1-8, 2013.
- [6] Imes Connor, Kim David H.K, Maggio Martina, Hoffmann Henry, "POET: a portable Approach to minimizing energy under soft real time Constraints," 21<sup>st</sup> IEEE Real time and embedded technology and application Symposium, pp. 75-86, 2015.
- [7] Sheikh.H.F. and Ahmad.I, "Simultaneous Optimization of Performance, Energy and Temperature for DAG Scheduling in Multicore Processors," International Green Computing Conference, pp.1-6, June 2012.
- [8] Sheikh.H.F and Ahmad.I, "Fast Algorithms for Thermal Constrained Performance Optimization in DAG Scheduling on Multi-Core Processors," 2011 International Green Computing Conference and Workshops (IGCC), pp.1-8, 25-28 July 2011.
- [9] Mohammed.R.K, Sahan.R.A, Prabhugoud.M, "Design Challenges of thermal margining tools for Silicon Validation" 12<sup>th</sup> Intersociety conference on,pp.1-8,2010
- [10] Ajami.A.H, Banerjee.K, and Pedram.M, "Modelling and Analysis of Nonuniform Substrate Temperature Effects on Global Ulsi Interconnects," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 6, pp. 849-861, June 2005.
- [11] Brest.J, Zumer.V, "A Performance Evaluation of list scheduling heuristics for task graphs without communication costs" Parallel processing, proceeding International workshop on , pp.421-428, 2000.
- [12] Zhou.J, Wei.T, Chen.M, Yan.J," Thermal Aware task scheduling for energy minimization in heterogeneous real time MPSOC system" IEEE Transaction on Computer Aided Design of Integrated circuits and system, pp-1, Nov 2015
- [13] Viswananth.R, Wakharkar.V, Watwe.A, and Lebonheur.V, "Thermal Performance Challenges from Silicon to Systems," *Intel Technol. J.*, Q3, vol. 23, p. 16, 2000.
- [14] Kwok Yu Kwong, Ahmad.I" Dynamic Critical Path scheduling: An effective techniques for allocating task graph to multiprocessor" IEEE Transaction on Parallel and Distributed System, vol-7,pp 506-521, Aug 2002
- [15] Gui.J, Maskell D.L "A Fast High level event Driven Thermal Estimator for Dynamic Thermal Aware Scheduling" IEEE Transaction on Computer Aided Design of Integrated circuits and systems, vol 31, pp 904-917, June 2012.
- [16] C. Hsu and W. Feng. A power-aware run-time system for high- performance computing. In Proceedings of the 2005 ACM/IEEE conference on Supercomputing. IEEE Computer Society washing ton, DC, USA, 2005.
- [17] Qinghui Tang, Sandeep K. S. Gupta, and Georgios Varsamopoulos. Energy-Efficient Thermal-Aware Task Scheduling for Homogeneous High-Performance Computing

Data Centers: A Cyber-Physical Approach. IEEE Trans. Parallel Distrib. Syst., 19(11):1458-1472, 2008.

- [18] Power Consumption curve of an Intel Core i7 950 CPU diagram, [http://www.xbitlabs.com/articles/cpu/display/power-consumption-overclocking\\_11.html](http://www.xbitlabs.com/articles/cpu/display/power-consumption-overclocking_11.html), June 3, 2016

#### Authors Profile

Er. Prabhjot Kaur pursued Bachelor of Engineering from Guru Nanak Dev Engineering College, Ludhiana India in 2013. I am currently pursuing M.Tech in Department of Computer Science and Engineering, Amritsar College of Engineering And Technology, India. Her interests include Multicore processor in Green Computing.



#### Authors Profile

Er. Manoj Agnihotri pursued Bachelor of Engineering from Beant College of Engineering and Technology, Gurdaspur India in 2005 and Master of Technology from Guru Nanak Dev University, Amritsar India in 2009. He is currently pursuing PhD from I.K Gujral Punjab Technical University and currently working as associate Professor in Department of Computer Science and Engineering at Amritsar College of Engineering And Technology, India. He has 7.5 years of teaching experience. His main research work focuses on Cloud Computing, Computer Algorithm And Green Computing.

