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Improved stability and access time Using Different 6T SRAM Cells at Low Voltage

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***Abstract*—** Contradictory nature of read and write stability and stability with speed necessitates the use of FinFET device which has less statistical variability, sensitivity and more on current. In this work, we explored three different FinFET device structures. These structures are used to form three different 6T SRAM cells. All the simulations are done with the help of Sentaurus TCAD. Three SRAM cells are compared to reduce access time and enhance data stability. We found that ADSE FinFET SRAM achieve significant improvement in access time as compared to Underlap FinFET SRAM cell without degradation of cell stability. On the other hand High-k spacer SRAM cell shows noteworthy increase in stability over other two cells with somewhat slower response.

***Keywords*—** ADSE, FinFET, High-k spacer SRAM, Underlap.

I. INTRODUCTION

SRAMs continue to be very important component and used for a wide range of microelectronics applications. It is used from consumer wireless to high performance server processors, multimedia and System on Chip (SOC) applications. Furthermore, cache memory demand is increasing in modern computer system since we are using multi-core architecture based microprocessor systems. In modern processors, the inbuilt memory is reaching almost 90% of total chip area and account for the significant amount of the chip area as well as power consumption. Since processor speed is increasing so the memory should be compatible with the speed of processor. Thus a well-designed SRAM cell should have high stability and high integration density. But stability and integration density could not improve together as both are competing parameters in SRAM cell design. Increasing the stability usually requires increasing the size of the SRAM cell, which decreases the integration density. For example, increasing the read SNM requires the drive strength of the pull-down (PD) transistor to be higher than that of the access (AC) transistor [1], which is often achieved by increasing the width of PD. Similarly decreasing the drain voltage to reduce dynamic power consumption result in lower static noise margin in read and write mode.

Any method to decrease the cell area increases the integration density of the chip and reduction in supply voltage reduces the dynamic power consumption, which potentially decreases the cost. Furthermore conflicting nature of read and write operation in 6T SRAM cell [2] with low supply voltage makes it highly challenging to design robust SRAM cell with high speed and good noise margins for the data stability in read, write and hold mode. Thus a SRAM cell is needed to be designed taking care of these issues so that we can get a stable cell without compromising integration density of chip.

In this work we explore device optimization for 20 nm FinFET based 6T SRAM cell considering the short channel effects. We determine the cell stability in read, write and hold mode. Using different FinFET structures we compared the stability and access time of SRAM cell in read and write mode. Asymmetric access transistor [3] SRAM cell is used to improve the read and write delay in read and write mode. Underlap FinFET [4], Asymmetric drain spacer extension FinFET [5], High-k spacer FinFET [6] structures are used and using these different noise margins and access time are compared for SRAM cell. Density gradient quantum correction model (for SCEs in nanometer region, doping dependent mobility correction in source-drain), PhuMob (for mobility degradation due to both impurity scattering and carrier-carrier scattering), Trap assisted tunneling model (for high k dielectric here HfO2), Oldslotboom model (BGN model) are used for the simulation of FinFET. The remainder of paper is organized as follows: Section II describes the FinFET device structures used to form the SRAM cell.

Section III gives the description of cell size issue in SRAM cell and size optimization in FinFET device structure. Section IV is concentrated on the structure of three SRAM cells used in this paper. In section V results obtained for the stability and delay are discussed and finally they are concluded in section VI.

II. DEVICE STRUCTURES

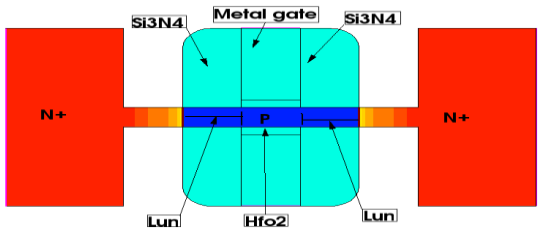
The electrical and physical characteristics of different FinFET structures used for SRAM design are described in this section. All the simulations are done on 0.5V supply with 0.3V as threshold voltage.

A. Symmetric-Underlap FinFET

We have simulated a 2d Underlap FinFET with 20nm gate length (Lg), 10nm fin thickness (Tfin), 0.75nm effective oxide thickness (TEO) and 40nm metal gate thickness (Tg). Source/Drain and Lext doping is kept 1020/cm3 with Gaussian profile and channel and underlap regions are undoped. FinFET with undoped underlap regions (Fig.1a) shows higher on current since gate underlap cover the fringing field lines from the gate electrode which terminate in these underlap regions in source/drain side. The thickness (TG) of gate electrode modulates the barrier in this region. Due to this barrier lowering in the underlap regions more carriers from the source enter into the channel region [7], resulting in higher Ion. Due to the undoped underlap regions random dopant fluctuation improves and which is good for stability of SRAM cell.

Table 1- Device Parameters

Parameter	Value
Gate length	20 nm
Fin Thickness (Tsi)	10 nm
Effective Channel Length	40 nm
Effective Oxide Thickness	75 nm
Channel Doping	1x1015 cm-3
Drain/Source Doping	1x1020 cm-3
Gate Work Function(N-FinFET)	4.4eV
Gate Work Function(P-FinFET)	4.9eV
Drain side spacer Length in ADSE FinFET	12 nm
Source side spacer Length in ADSE FinFET	8 nm
Underlap Length (Lun)	10 nm
VTH	0.3 V
VDD	0.5V



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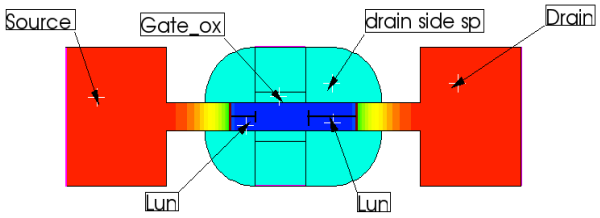

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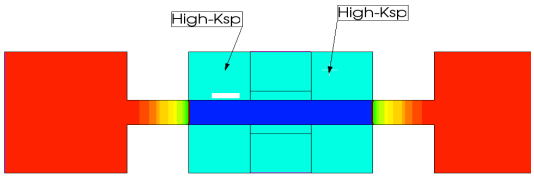

C

Figure.1 Top Cross sectional view of- (A) Underlap FinFET. (B)ADSE FinFET and (C) High-kS FinFET

B. Underlap FinFET with asymmetry

For this structure all the dimension are same as used for symmetric Underlap FinFET except spacer. Source side spacer is kept at 8nm and drain side spacer is extended by 4nm but overall device dimension is kept constant to symmetric Underlap FinFET. Underlap region is kept constant but shifted in drain side. In other words the structure is asymmetric underlap with asymmetric spacer. FinFET with asymmetric drain spacer and underlap (Fig.1b) improves the short channel characteristics because the increase in drain side spacer which makes gate control over channel better in this side of channel length. An asymmetry is created between source to drain (ISD) and drain to source (IDS) current because of the extra underlap. The structure also shows better on current.

Table 2. Various device parameters for different FinFET structures

No.	1	2	3
Device	**Underlap FinFET**	**Underlap FinFET(ADSE)**	**Underlap FinFET (H-kS)**
I_{on}/I_{off} (10^4)	300	5	68.8
SS (mV/Dec.)	58	66.5	60
DIBL (mV/V)	11	20.25	6

C. Underlap FinFET with High-k spacer

All the dimension of this structure is also kept same as Underlap FinFET. Underlap is covered with high-k spacer (HfO2). Drain current to gate voltage curve of three structures is given in Fig.2. FinFET with high-k spacer

(Fig1.c) is more immune to random statistical variation [8] thus gives better short channel characteristic`s. Due to enhance fringing field of high-k spacer as carriers comes near surface they become highly concentrated [9], leads to less variation in Ion. Important parameter related to all three structures is given in the table II.

III. SRAM SIZE CONSIDERATION

In FinFET design fin thickness is important parameter to be considered. Natural length (ƛ) is the parameter measures the short channel effects and depends directly on fin and oxide thickness. It represents the distance of penetration of drain electric field into the channel [10]. A small value of ƛ is desirable to minimize the SCE. For FinFET it is given by:

$$ƛ = [(Ɛsi /2Ɛox) (1+Ɛoxtsi/4Ɛsitox) tsi\ tox]1/2 \quad \text{……...(1)}$$

In case of SRAM in the read operation both BL and BLB are kept high at the beginning, it should be take care that read operation must not corrupt (un-intended flip) the value stored in the bit cell.

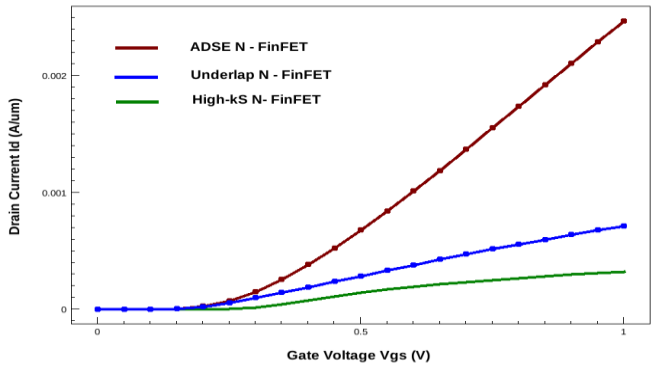

Figure.2 I_d-V_{gs} Characteristics of different FinFET structures.

In order to avoid the un-intended flip of the value, it is desirable to keep the voltage at the internal node below the trip point of the inverter which has a stored value of '0'. So strength of the pull-down transistors should be more than the strength of the access transistors for a non-destructive read operation. Similarly, for a successful write operation, it is desirable to bring down the voltage of the internal data storage node Q (or QB) in which value '1' has been stored, below the trip point of the inverter. Therefore, pull-up transistors must be weaker than the access transistors for a constructive write operation. Combining these constraints, transistors strength has the following relation:

Strength of Pull-up < Access < Pull down

In our simulation cell ratio (W/LPD)/ (W/LACC) is taken as 1.5 and pull ratio (W/LPU)/ (W/LACC) is taken as 1.

IV. FINFET SRAM CELLS

In this section three different 6T SRAM cells used to compare the read and write operation are described. In the first cell (named Underlap FinFET SRAM) all six transistors used are Underlap FinFET. Transistors are sized minimum to take care of chip integration density.

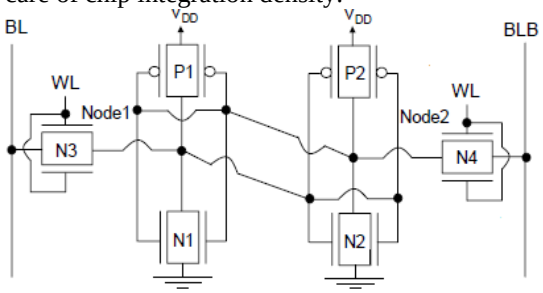

Figure.3 6T SRAM cell [11]

In the second cell (named ADSE FinFET SRAM) asymmetric drain spacer and underlap FinFET device is used for access transistor. Pull up and Pull down transistor is made of Symmetric-Underlap FinFET device structure.

In the third cell (named High-k FinFET SRAM) all six transistors used are Underlap FinFET with High-K (HfO2) spacer.

V. SRAM SIMULATIONS

The read and write stability and access delays of three SRAM cells are compared in this section for a 20 nm FinFET technology using Sentaurus TCAD.

A. Read and Write mode stability

Static noise margin (SNM) calculation using butterfly curve, is the metric used to characterize the stability of SRAM bit cell in this paper. The SNM is defined as the maximum amount of DC noise (VN) that can be introduced in the cross-coupled inverter pair such that the bit cell retains its data before flipping. From the butterfly curve we calculate the maximum size square to calculate the SNM, and minimum of two is taken as SNM. SRAM cell with Symmetric FinFET shows good RSNM but SRAM cell with High-k spacer shows 29% more SNM than the earlier due to the superior electrostatics and enhance gate control to the channel. As carriers become highly concentrated near the surface, leads to less variation in Ion. On the other hand ADSE FinFET SRAM cell show negligible variation in stability and is slightly less than the Underlap FinFET SRAM cell.

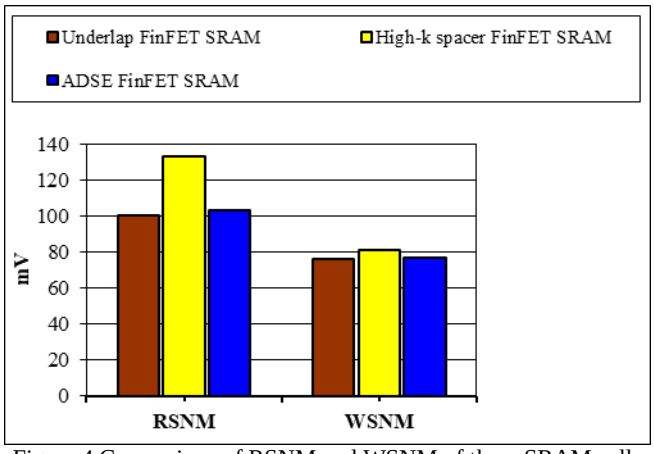

Figure.4 Comparison of RSNM and WSNM of three SRAM cells

In case of WSNM high-k spacer SRAM cell has 7% improvement in comparison to Underlap FinFET SRAM and ADSE SRAM cell shows 3% improvement. Due to the ADSE access transistor become slightly stronger than in the normal Underlap FinFET, which is the possible region for this slight increment. RSNM and WSNM results of all three SRAM cell are shown in Fig.4.

B. Read and Write delay

During read operation fight occurs between pull down and access transistor. Pull down transistor needs to be stronger than access transistor for better read operation while access transistor should be stronger than pull up transistor for write operation. ADSE FinFET SRAM cell has 42% improvement

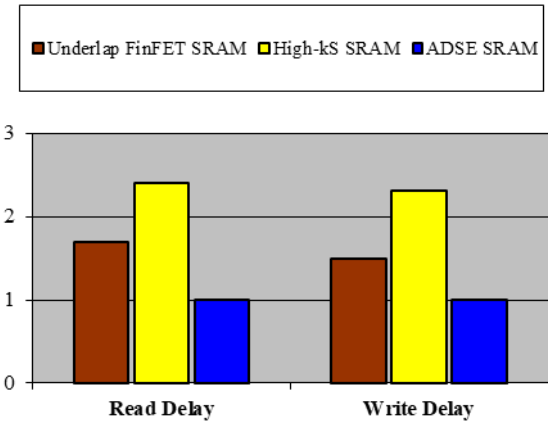

Figure.5 Normalized value of delay in read and write mode of three SRAM cell

in the read delay as compared to Underlap FinFET SRAM cell. Due to the asymmetry in ISD and IDS current in ADSE FinFET, read current enhance in drain to source direction when drain is connected to higher voltage in read operation. Actually in this situation gate has better control in source side. In case of write operation drain is connected to lower voltage side and hence current from source to drain increase since now gate has better control in drain side. Thus in write mode ADSE FinFET SRAM cell gives 34% more speed than Underlap FinFET SRAM cell.

While Underlap FinFET SRAM cell has 29% and 35% improvement in delay performance over High-k spacer FinFET SRAM cell in read and write mode respectively. This is because on current decrease due to mobility degradation in Dual-k spacer FinFET. As this structure has intense longitudinal electric field carrier mobility degrades near surface. Fig.5 shows the read and write, mode operation delay of three FinFET SRAM cells.

VI. CONCLUSION

Three FinFET SRAM cells are compared in this paper on the basis of read, write data stability and the memory integration density while reducing the access time of operations. We found that Underlap FinFET SRAM and ADSE FinFET SRAM cell has almost same stability in read and write mode but High-k spacer SRAM cell is found to be most stable among three. Read stability (RSNM) is very much improved in comparison to other two. Symmetric U- FinFET SRAM cell has more read and write delay than ADSE FinFET SRAM cell but less than High-k spacer SRAM cell. In case of delay difference of three SRAM cells can be easily visualized. So High-k spacer SRAM cell can be better in low power application and ADSE SRAM cell in high speed operations while Underlap FinFET SRAM cell is compromise of both.

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