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28nm FPGA HSTL IO Standard Green RS Flip Flop Design for AI Based Processor

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***Abstract*—**The flexible, reusable nature of FPGAs makes them a great fit for different applications, from driver development to data processing acceleration. FPGAs can be programmed for different kinds of workloads, from signal processing to deep learning and big data analytics. In this article, we focus on the use of FPGAs for Artificial Intelligence (AI) workload acceleration. To make this thing happen we have design FPGA based Flip Flop Design for AI Based Processor. Here we have designed energy efficient RS Flip Flop. In consideration of technology upgradation, we have used 5G frequency for calculating total power consumption from 1GHZ to 5 GHZ. We have used two different IO standard HSTL_I_12 and HSTL_II_18 with different voltage (0.970, 1.009, 0.986 and 0.998 Volt). During the experiment we have found by applying HSTL_I_12 we have reduced our total power consumption by 44.87% which is significant among all the analysis.

***Keywords*—** FPGA, AI, HSTL, flip flop, 28nm.

I. INTRODUCTION

In digital electronic Flip flop is a circuit device that used to store two stable state information that is also called bistable multivibrator. It changes its state at one or more input with one or more output. Flip flop has huge advantage in computer system and digital communication system. It is basically referred as storage element in sequential logic.

The clocked RS Flip flop consist of a basic NOR Gate & two AND Gate. In table 1 we have shown that as long as the clock pulse is 0 then output would be 0 regardless the S and R" input values. when clock pulse will be 1 information is allowed to reach the basic RS flip flop with different (0&1) output.

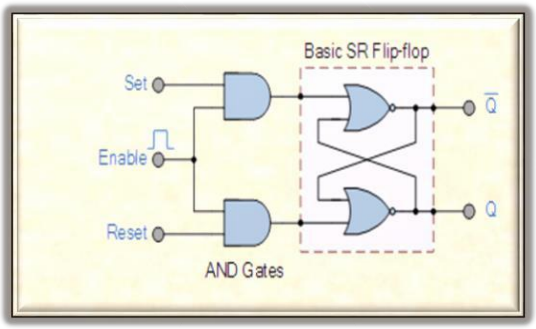

FIG.1 Circuit Diagram of RS Flips Flop

In figure 1 we have shown a basic flip flop which stand as an asynchronous sequential circuit, having a set of input (S) and reset input (R) and clock pulse is enabled.

In table 1 we have shown the truth table of RS flip flop.

S	R	Q	Q'
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

FIELD PROGRAMMABLE GATE ARRAYS (FPGAs) is an integrated circuit (IC) that can be programmed in the field after manufacture. Which is replacement of ASIC technology ASIC stands for application specific integrated circuit. In ASIC once our requirement would change then we do not have any scope to redesign it or reprogrammed the chip. In contrast in FPGA we can modify it with reprogrammed it. To reprogrammed the chip basically there is two language VHDL and Verilog.

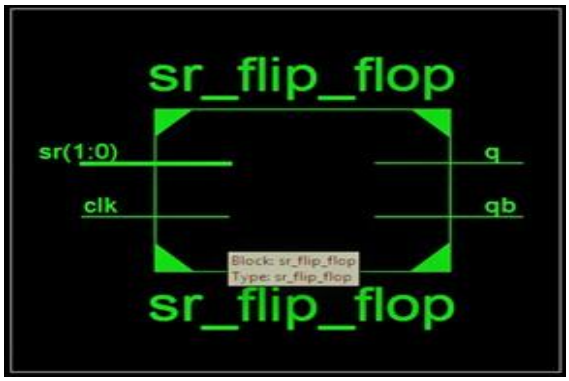

Fig.2 SR Flip Flop

In our work we have deigned our RS flip flop by using Verilog language.

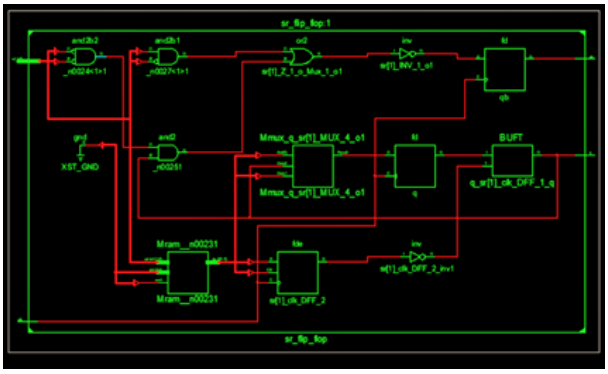
Fig3. RTL Schematic

II. RELATED WORK

In our research, we come across with many direct applications of HSTL in energy efficient design like power consumption [1], one-bit store flip flop [2]. [3], energy efficient design and implementation of processor [4]RS flip flop [5]. IO standards were also used in energy efficient design of 28nm FPGA [6]. There are many low power techniques. Those are widely used in practice for design of digital system [7]. Power consumption analysis of AI based technology [8] in this work. HSTL IO Standards Based Processor Specific RS flip flop [9]. Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in processor on kintex-7 FPGA [10].

III. METHODOLOGY

1.1 FPGA METHODOLOGY:

The Xilinx FPGA based device procedure in figure4 allows to attain the optimality of device and design features, such as:

- ✓ Routing Operation
- ✓ Design Performance
- ✓ Lower Power requirement
- ✓ Higher accuracy processing

This procedure too allows toward attain productivities in:

- ✓ Software runtime
- ✓ Debugging ability
- ✓ Movability

During the design of the component

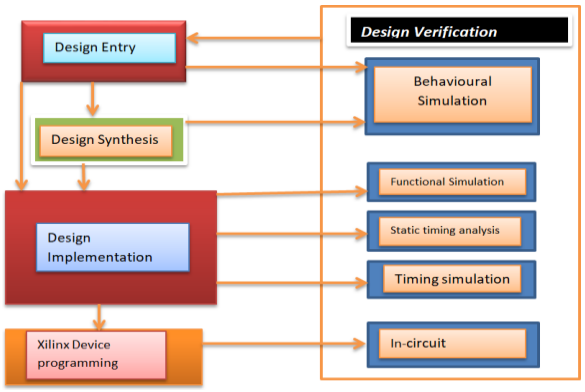

Figure 4. FPGA Methodology

In this work we have design FPGA base RS flip flop using the Verilog. During the work first we have work with the RTL design, register-transfer level is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals. After that Behavioral design completed here, we have verified syntax and functionality without timing information. Later we have performed gate level simulation in post synthesis simulation. In last we have done post implementation simulation.

IV. RESULTS AND DISCUSSION

Table 1: Calculating total power by applying HSTL_I_12 IO standard at 0.970Volt

Frequency	Clock	Signal	IO	Leakage	Total
1 GHz	0.004	0.000	0.015	0.077	0.097
2 GHz	0.008	0.001	0.019	0.077	0.105
3 GHz	0.013	0.001	0.025	0.077	0.113
4 GHz	0.017	0.002	0.025	0.077	0.121
5 GHz	0.121	0.002	0.029	0.077	0.129

In table 1 we have used HSTL_I_12 IO standard at .970 Volt by changing the frequency from 1GHZ to GHZ. During the experiment we have found that Leakage power was constant and found big change in clock power. When we change the frequency from 5GHz to 1GHz we reduced the energy consumption to 24.80%. Same data we have shown in figure 5 by graph.

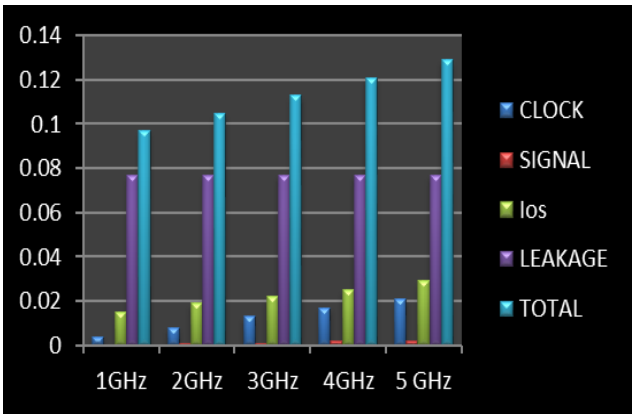

Fig5. Graph of table1

Table 2: Calculating total power by applying HSTL_I_12 IO standard at 1.009Volt

Frequency	Clock	Signal	IO	Leakage	Total
1 GHz	O.004	0.000	0.016	0.080	0.100
2 GHz	0.009	0.001	0.019	0.080	0.108
3 GHz	0.013	0.002	0.022	0.080	0.117
4 GHz	0.018	0.002	0.026	0.080	0.125
5 GHz	0.022	0.003	0.029	0.080	0.133

In table 2 we are working with HSTL_I_12 IO standard at 1.009Volt with frequency 1GHz to 5Ghz. Here we have found when we change the frequency form 1GHz to 5GHz we got 44.82% reduction in total IO power. In total power consumption we reduced the total power consumption by 24.81%. Same result we shown in figure 6.

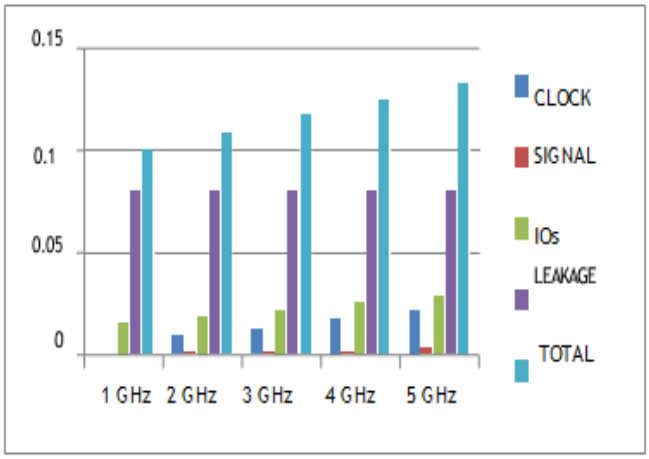

Fig.6 graph of table2

Table 3: Calculating total power by applying HSTL_II_18 IO standard at 0.986Volt

Frequency	Clock	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.020	0.079	0.104
2GHz	0.010	0.000	0.027	0.079	0.115
3GHz	0.015	0.000	0.033	0.079	0.127
4GHz	0.019	0.001	0.031	0.079	0.138
5GHz	0.024	0.001	0.046	0.079	0.150

In table 3 now we changed our IO standard HSTL_I_12 IO standard to HSTL_II_18 IO standard at voltage 0.986Volt. During the experiment we have found that when we altered the frequency from 5 GHz to 1 GHz found 30.67% in total power consumption. In figure 7 we have discussed same analysis.

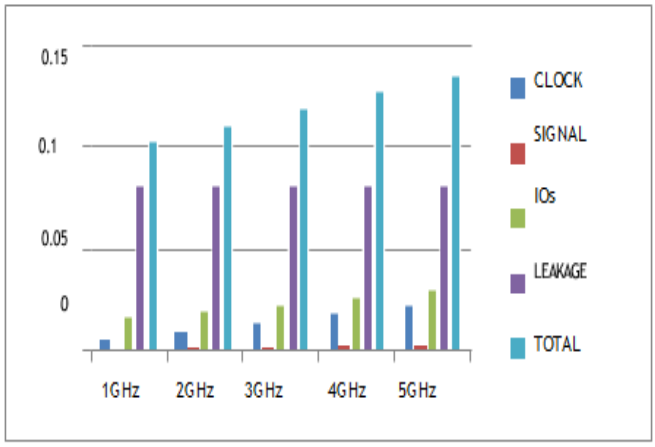

Fig7.graph of table3

Table 4: Calculating total power by applying HSTL_II_18 IO standard at 0.998Volt

Frequency	Clock	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.020	0.079	0.105
2GHz	0.010	0.000	0.027	0.079	0.117
3GHz	0.015	0.000	0.033	0.079	0.128
4GHz	0.020	0.001	0.039	0.079	0.140
5GHz	0.025	0.001	0.046	0.079	0.151

In table 4 for calculating total power consumption we applied HSTL_II_18 IO standard at 0.998Volt. Here we found no change in signal and leakage power. While fluctuating the frequency from 5GHz to 1GHz we reduced the total power consumption to 30.46%. Same analysis we have elaborated with figure 8.

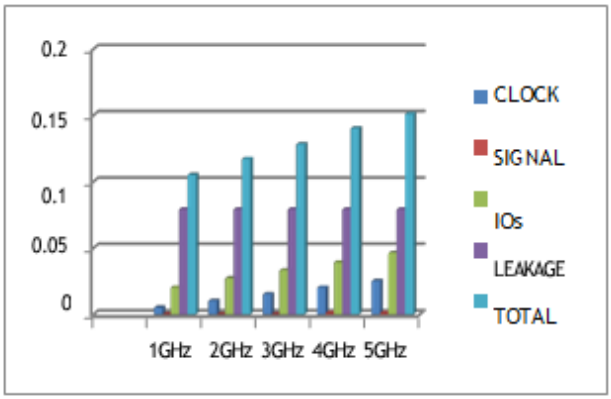

Fig8. Graph of table4

V. CONCLUSION

In our research our main objective is to calculate total power consumption of FPGA based RS Flip Flop. For the analysis we have consider diverse voltage like 0.970volt, 1.009Volt, 0.986Volt and 0.998volt. We have also used two different IO standard HSTL_I_12 and HSTL_II_18. For calculating total power, we have four different parameters like Clock, Signal, IOs and Leakage power. In our experiment we have found best result through table 2. Here when we change the frequency from 5Ghz to 1Ghz then we reduce the power consumption by 44.82%.

VI. FUTURE SCOPE

In this work, we have implemented on KINTEX-7 (family), we can redesign this component on other new family of FPGA like VIRTEX7 and ARTIX7 and measure the power consume efficiently.

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