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Performance Analysis of Array Multipliers Using Different Logic Configurations

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Abstract - Power and speed are the two important design aspects that impact the designing of any circuits. One of the most widely used arithmetic operation in digital circuits is Multiplication. There are different Multipliers designed depending on the speed and the hardware. There are different technologies with different features. In this paper 4- bit and 8- bit Array Multipliers are been designed using different designing techniques. The Multipliers are designed using CMOS Logic Configuration, Pseudo-NMOS Logic Configuration and Transmission gate Logic Configuration and are compared in terms of Power and delay. The Power Delay Product (PDP) gives the overall performance of the Multipliers.

Keywords - Multiplier, CMOS Logic, Pseudo-NMOS Logic, Transmission Gate Logic, Power, Delay.

I. INTRODUCTION

Multiplication plays an important role in digital circuits. Adders and Multipliers are the two basic building blocks of any digital circuits. The two basic operation of Multiplication process is:

1. Generation of Partial Products.
2. Accumulation of the products.

The basic Multiplication process is the add and shift algorithm. The partial products are generated using the AND gates and these products are accumulated using the adders. Therefore by reducing the number of partial products or by accelerating the accumulation the multiplication operation can be speeded up. In this paper the Multipliers are constructed using CMOS, Pseudo-NMOS, and Transmission Gate logic configuration and are compared in terms of power and delay.

The paper is organised as follows: Section II provides the introduction for designing the Multipliers. Section III gives the various designing algorithms. The Power dissipation details are provided in Section IV. Comparison of the Multipliers based on different designing techniques is shown in Section V. Section VI gives out the final conclusion based on results obtained.

II. MULTIPLIER & DESIGNING

Multipliers play an important role in arithmetic operations. They are most commonly used in Arithmetic and Logic units, Filters, DSP applications, Processors.

A. Array Multipliers

The array Multiplier originates from the multiplication parallelogram. Multiplier is based on the add and shift on multiplication of the multiplicand with one multiplier bit. The length of the multiplier is represented by the number of rows and the width of width of each row represents the width of the multiplicand. The parallel adders receive the partial product inputs and the carry out is propagated into the next rows. The critical path delay consists of the horizontal and vertical terms. This delay consists of both adder delay and gate delay. The basic block diagram of 4 bit multiplier is shown in fig 1.

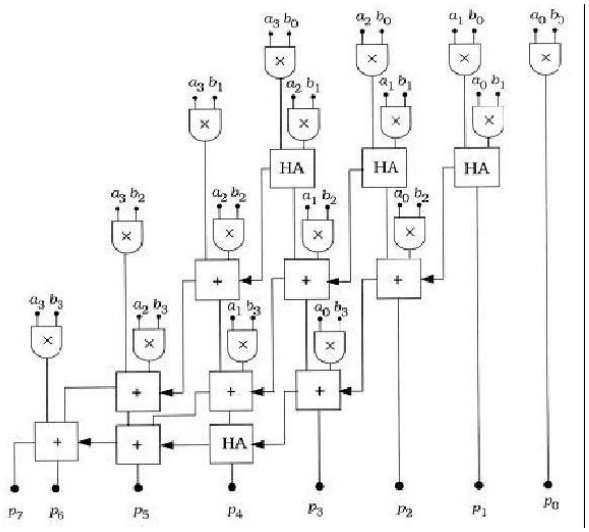

Fig 1. 4 bit unsigned array Multiplier.

The advantage of using an array Multiplier is its regular structure which makes it easy to layout and small in size. The design time is much faster than the tree multiplier. The speed will be low for very wide multipliers.

III. DESIGNING ALGORITHMS

There are a number of designing techniques used for designing the digital circuits. In the present paper we design the Multiplier using three different logic. Here the considerations on power, the logical working are discussed further.

A. CMOS Logic Configuration

CMOS circuits use a combination of p-type and n-type transistors to implement logic gates and other circuits. This technology is used in microprocessors, microcontrollers, static RAM and other digital logic circuits. The two important characteristics of CMOS devices are high noise immunity and low static power consumption. It always uses all Enhancement MOSFETs. The overall circuitry requires very high transistor count. A complementary MOSFET (CMOS) full adder is designed by using pull up and pull down networks .Here the CMOS adder uses 28 transistors where they are highly efficient due to complementary transistor pairs. The voltage scaling and high noise margin design makes them highly advantageous than others thus it makes them to work at low voltages at ratio less transistor sizes. Figure 2 shows the AND gate circuit.

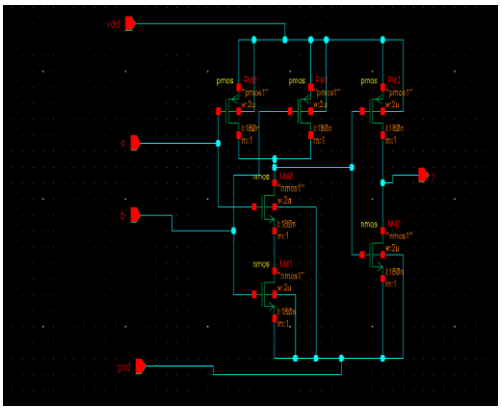

Fig 2.AND Gate using CMOS Logic

B. Pseudo-NMOS Logic Configuration

The name Pseudo-NMOS originates from the older NMOS techniques where a depletion mode NMOS transistor with its gate connected to source was used as a pull up device. Here the PMOS transistor simply acts a pull up device for an n-block. The PMOS is always ON since the gate is grounded. It is advantageous since it provides high speed with low transistor count, but on the negative side more power consumption because of the pull-up transistor, reduced output voltage swing and gain. Figure 3 shows the AND gate circuit.

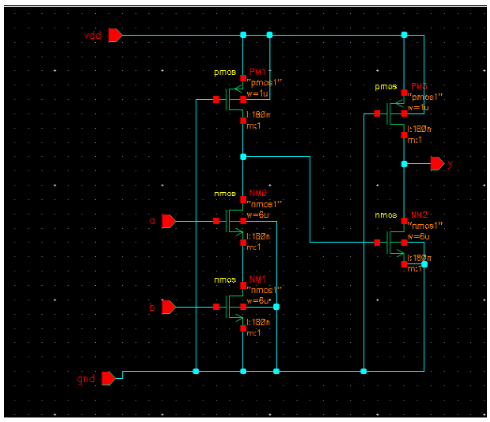

Fig 3.AND Gate using Pseudo-NMOS Logic

C. Transmission Gate Logic Configuration

A Transmission gate is similar to a relay that can conduct in both directions. It is a CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1.Here both PMOS and NMOS work simultaneously. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition of the resistance curves of the two transistors.

Figure 3 shows the AND Gate circuit.

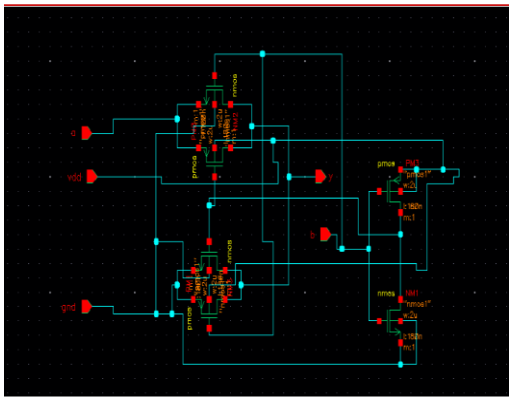

Fig 3.AND Gate using Transmission Gate Logic

IV. POWER DISSIPATION

The switching activity of the circuit and the node capacitances determines the Power dissipation. The wiring complexity is determined by the number of connections and their lengths. These characteristics vary from one design technique to other. Therefore proper choice has to be done for considerable circuit performance. The Power consumption is said to have three components which are termed as:

- Switching Power: consumed in charging and discharging of the circuit capacitances during transistor switching.

- Short-Circuit Power: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.
- Static Power: consumed due to static and leakage currents flowing while the circuit is in a stable state.

The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology.

V. SIMULATION RESULTS & COMPARISON

The 4-bit and 8-bit Array Multipliers are constructed using the three design techniques as mentioned. They are compared in terms of Power, Delay and PDP. The circuits are designed using Cadence tool using 180nm technology for obtaining better performance.

Table I gives the comparison of the multipliers

Figure 4 gives the input waveform and Figure 5 shows the output waveforms of four bit Array Multiplier.

Figure 6.a and 6.b gives the input waveform and Figure 7 shows the output waveforms of eight bit Array Multiplier.

Table I. Comparison of Array Multipliers.

Array Multiplier	CMOS			Pseudo-NMOS			Transmission Gate		
	Power (W)	Delay (s)	PDP	Power (µW)	Delay (s)	PDP	Power (µW)	Delay (s)	PDP
Four Bit	288.9 $x10^{-6}$	132.0 $x10^{-12}$	38.134 $x10^{-15}$	30.38 $x10^{-3}$	68.82 $x10^{-12}$	2.090 $x\ 10^{-12}$	2.811 $x10^{-3}$	123.3 $x10^{-12}$	346.59x 10^{-15}
Eight Bit	1.889 $x10^{-3}$	116.4 $x10^{-12}$	219.87 $x10^{-15}$	149.4 $x10^{-3}$	95.49 $x\ 10^{-12}$	14.266 $x\ 10^{-12}$	16.84 $x10^{-3}$	116.2 $x\ 10^{-12}$	1.9568x 10^{-12}

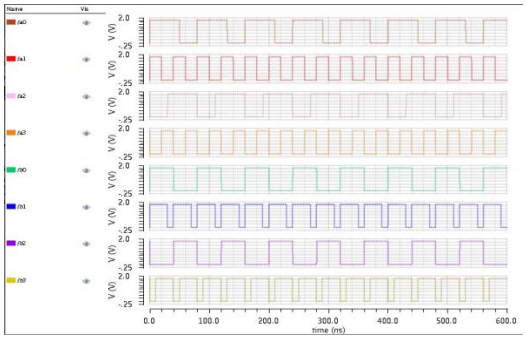

Fig 4. Inputs of four bit Array Multiplier.

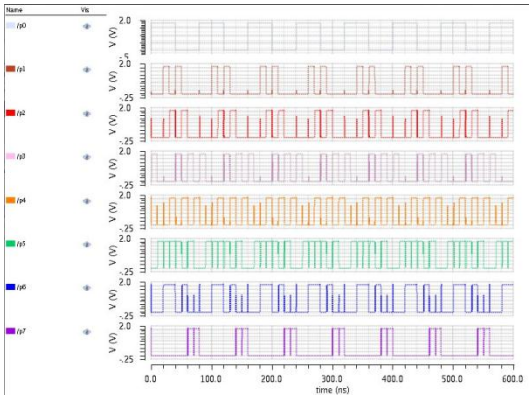

Fig 5. Outputs of four bit Array Multiplier

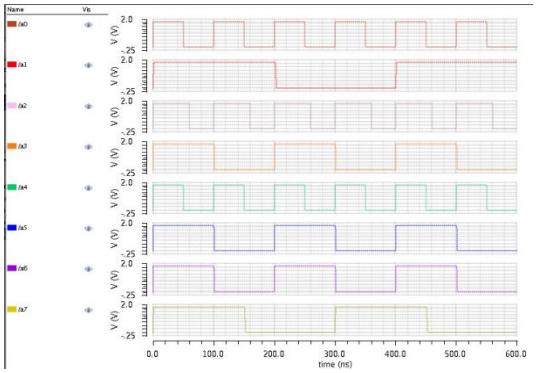

Fig 6.a. Inputs (a0 to a7) of eight bit Array Multiplier

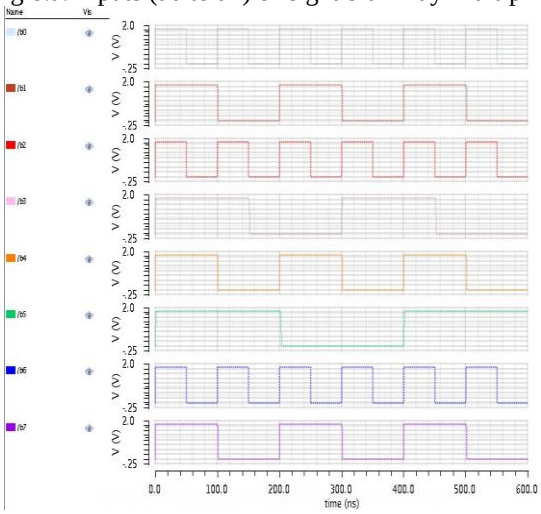

Fig 6.b. Inputs (b0 to b7) of eight bit Array Multiplier.

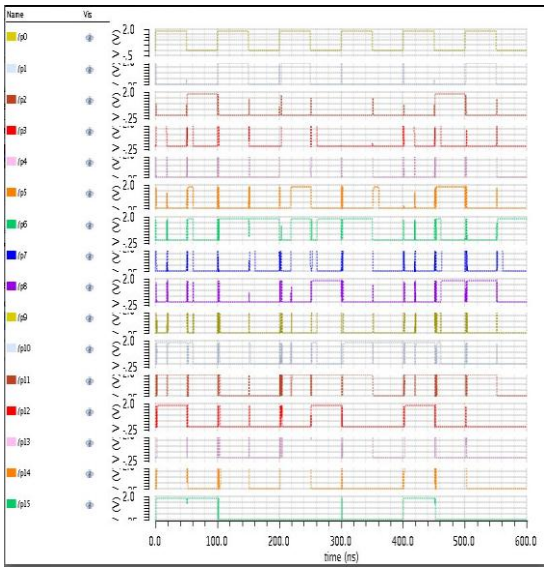

Fig 7. Outputs (p0 to p15) of eight bit Array Multiplier.

VI. CONCLUSION

The array multiplier is implemented by different low power techniques namely CMOS, Pseudo-NMOS and Transmission Gate techniques. The results are simulated using cadence and comparison has been done for different parameters like power dissipation, delay and PDP. The results concluded that as compared to other proposed techniques, CMOS has less delay and PDP. These advantages of proposed techniques make CMOS more efficient and convenient to be used in digital circuits.

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