IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-7, Issue-10, Oct 2019 E-ISSN: 2347-2693

The First Six-Core Intel Xeon Microprocessor

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DOI: https://doi.org/10.26438/ijcse/v7i10.198200 | Available online at: www.ijcseonline.org

Accepted: 12/Oct/2019, Published: 31/Oct/2019

***Abstract*—** This paper describes the next-generation Intels Xeons microprocessor designed for a broad range of highly power-efficient servers, codename Dunnington. The Dunnington processor has six cores (three core-pairs) integrated with large, dense, on-chip caches, and it delivers the dramatic power efficiency of Intel's 45nm high-K metal gate process and the Intel Core 2 microarchitecture to server platforms. This processor implements a high bandwidth-dedicated interface from each of the three core pairs to the last-level cache (LLC) for the effective use of the inclusive LLC. With high functional integration, large cache size, and 1.9 billion transistors, the processor's moderate server-class die size of 503mm2 is achieved by optimizing the floor plan and physical design. Thermal Design Power (TDP) limits of 50, 65, 90, and 130W. This processor will be the first part to employ core recovery techniques for reducing product cost

Keywords*—Xeon, six cores, Dunnington, 45nm*

I. INTRODUCTION

The high-performance expandable server processor market segment has witnessed ever-increasing demands for throughput performance and energy efficiency. To meet these demands we focused on intelligent integration of multiple cores for power efficient parallel computing to deliver increased performance. The key high-level design requirements for the next-generation Intel's Xeons microprocessor, codename Dunnington, Intel's latest offering in this segment, were a drop-in replacement compatibility with its predecessor, Intel's Dedicated High Speed Interconnect (DHSI)-based quad-core processor, codename Tigerton, on the Caneland platform; a 30percent boost in performance over its predecessor; and operation in the range of 50–130W power envelopes. In addition, maintaining compatibility between different pools of machines and stacks of software is one of the major problems in data-center and server management. Hence, enhancing the virtualization support for load-balancing across computing pools was a critical feature requirement for the Dunnington processor. This is the first Intel six-core Xeon processor, integrating a three-level, on-chip cache hierarchy and a fast DHSI system interface slated for introduction in the second half of 2008. The requirement for integrating six cores and such a large Last-Level Cache (LLC) had profound implications on the physical and electrical design of the Dunnington processor. Significant among these were die size constraints, achieving bin-split targets for the different market segments, meeting reliability constraints due to the 1.9 billion on-die transistors, dealing with process variations across the large die, and meeting thermal envelope limits. In this paper, we describe each of these challenges and the solutions developed by our team to successfully bring the product to market ahead of schedule.

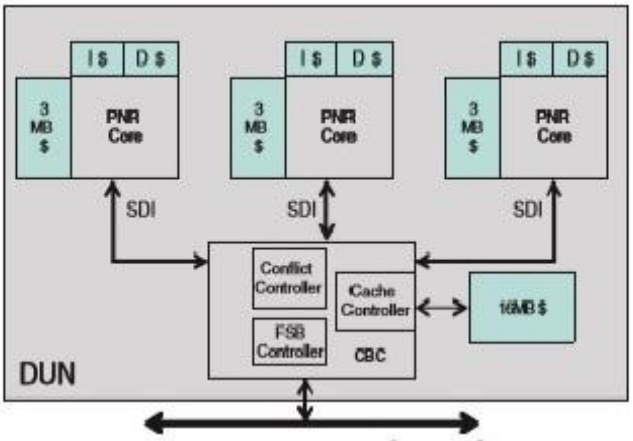

Figure I.1: Next-generation Intels Xeons processor architecture

II. RELATED WORK

In [1] this paper we have examined that with the added number of cores in a process generation, the overall power dissipation of the processor increases proportionally. This affects both the leakage power and the dynamic power components. The Dunnington processor, however, was required to fit multiple market segments, namely rack, blade and ultra-dense segments, which have TDP requirements of approximately 130, 90, and 60W, respectively. Initial

analysis of the microarchitecture indicated that the thermal envelope would be violated if steps were not taken to address the exposure. Power dissipation can be reduced by lowering the voltage with a commensurate reduction in frequency. However, the voltage cannot be reduced below the VCCmin target, because this may affect functional robustness. The VCCmin target is determined primarily by the overall spread of statistical variation [2] of all transistors in a power plane. Hence, operating voltage reduction to reduce power is an option only for VCCmin. This meant over 1.9 billion transistors are operated on a single power plane, which affects the VCCmin of the product considerably. Hence, further measures besides voltage lowering were required to fit the six cores, the large cache, and the Uncore into a thermal envelope of 130W.

In [2] this paper we explored that the Dunnington processor has three levels of caches: 32KB of data and 32KBs of instruction cache in each Penryn Core (First-Level Cache or FLC), 3MB of non-inclusive Mid-Level Cache (MLC) for each CMP core-pair, and 16MB of inclusive LLC. Inclusivity of the LLC is maintained using core valid bits per Penryn core-pair.
The Dunnington processor implements the joint MESI states of ES, MI, and MS
The MLC and LLC are safeguarded by Intel Cache Safe Technology. The MLC utilizes the Single Bit Fix (SBF) mechanism, while the LLC includes a cache line disable facility. These features address the cache reliability requirements of the server market segment.

In [3] this paper we studied that the technology used for design is innovative. One of the key innovations in the new 45nm process technology is the high-kþ metal gate transistor, which is one of the biggest changes in transistor technology since the introduction of the polysilicon gate MOS transistor in the late 1960s. The new 45nm process technology offers about a 2improvement in transistor density, approximately 20 percent of an improvement in transistor switching speed, or more than a 5reduction in the source-drain leakage. It also provides at least a 10 reduction in gate oxide leakage power and more than a 30-percent reduction in transistor switching power [1].

III. RESULTS AND DISCUSSION

We have analyzed that the high-performance expandable server processor market segment has witnessed ever-increasing demands for throughput performance and energy efficiency. To meet these demands we focused on intelligent integration of multiple cores for power efficient parallel computing to deliver increased performance. The key high-level design requirements for the next-generation Intel's Xeons microprocessor, codename Dunnington, Intel's latest offering in this segment, were a drop-in replacement compatibility with its predecessor, Intel's Dedicated High Speed Interconnect (DHSI)-based quad-core processor, codename Tigerton, on the Caneland platform; a 30percent boost in performance over its predecessor; and operation in the range of 50–130W power envelopes. In addition, maintaining compatibility between different pools of machines and stacks of software is one of the major problems in data-center and server management. Hence, enhancing the virtualization support for load-balancing across computing pools was a critical feature requirement for the Dunnington processor.

IV. CONCLUSION AND FUTURE SCOPE

The Dunnington processor team integrated six cores on a single die with a 25-MB cache to achieve a 30percent increase in performance over its predecessor on the same platform. This product has virtualization features that are critical on servers for datacenter applications. Performance per watt efficiency was accomplished with a low-leakage variant of the 45nm process technology to enable SKUs for high-performance, rack, and ultra-dense segments. Modular design and reuse of IP/methodologies during the entire design and validation cycles enabled a successful execution that beat the time-to-market window.

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