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Design of Resolver-To-Digital Converter for Motor Control Applications

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***Abstract*—** Prevalent Resolver to Digital Converter (RDC) is frequently adopted using DSP techniques to reduce the hardware tread and improve system accuracy. However, in such implementations, both resolver and ADC channel imbalance introduce significant errors, practically in speed output of the type-II track loop algorithm. This paper discusses the design of digital filters based on the interpolation of pre-design filters for a DSP based on type-II track loop algorithm with square wave excitation. Such filters are tenth order high pass filter and tenth order peak filter, the projected DSP based RDC system is executed in MATLAB/SIMULINK the simulation results demonstrate the decrease the peak-to-peck error estimation of speed out response of the system.

***Keywords*—** Resolver, RDC, type-II tracking loop algorithm, ADC channels, Adaptive digital filter design.

I. INTRODUCTION

The rotor Shaft-angle measurement is a most essential constraint in the modern control, and computing technologies. Resolver is a one type of transducer or sensor which estimates the immediate rotor angular position of rotating shaft which attached to it. The rotor shaft angle is used in measurement and control of position, velocity, and acceleration in systems. The shaft-angle transducers acquire the angular position of shaft and convert the mechanical movement into electrical signals. The angular position of rotor is to be extracted from the filtered output of the quadrature resolver signals. The accuracy achieved both position and/or speed measurement by the resolvers depends on the quality of the analog signals and on the determination of the digital converters used to combine resolver to the control units. This conversion is made by the resolver to digital converter (RDC).The simplicity of the resolver design makes them reliable extreme applications such as servo motors steel and paper mills, jet fuel systems, communication position systems. Aircraft surface actuators.

A resolver is transducer to measures angular position, which consists of one primary (i.e. rotor) winding and secondary (i.e. stator) windings. A resolver's contains two analog signal outputs such as SIN& COS are modulated by rotor excitation or carrier signal and RDC is always needed to improve the angular position in digital form using ADC channels. RDC perform demodulation of the resolver output of signals to take away carrier signal and determination of angle measurement to give digital form of the rotor shaft angle. There are two different methods are there such as Inverse tangent (open loop) and ATO or Type-II track loop techniques are mostly use for the design of RDC's with blow up of microprocessor technology, that is DSP technology. Progressively focused on software DSP based RDC techniques. Latterly: several researchers have shown interest to build up humble and low cost based RDCs.

The fast angle tracking based RDC use a phase comparator of type is bang-bang for angle tracking is proposed here used PLL technique [1]. Though this method not gives tracking errors at speed and out of lock conditions of the PLL, to be employed in applications like EMB system, to solve that problem proposed Recursive Least Square (RLS) deviate from the exact constraint values throughout low speed [2] it suffers from process during these arises when the brake pedal is in incessant contact with the bark disk tacking of the variations in resolver parameters with temperature is requisite for the actuator position control and its stability. Whereas other are software based tacking the shaft angle implemented the ATO based PLL techniques [3]. Which is probable angle measurement done through track the variations of the rotor shaft-angle. However, this sinusoidal envelop output signals are frequently disturbed by unexpected events are as dc- offset values. Proposed PWM conversion of ATO method such methods are not gives minimum tacking error output of demodulated signal [4]. To improve demodulation accuracy overcomes the influence of these factors, an automatic offline calibration method proposed for two sinusoidal envelop signals [5]. Virtually a resolver produces periodic position errors for the amplitude

imbalance. The special effects of the position errors are evaluated, in automobiles RDC's are used for detect the velocity and driving distance [6]. To solve this problem deals with method of Double Synchronous Reference Frame-Based Phased-Locked loop (DSRF-PLL) this method faced problem of down sampling with aliasing effect understating problem of DSP, the two sinusoidal orthogonal signals after envelop detector section [7]. A Pulse Width Modulation (PWM) technique is projected proposed predominantly for the decrease the destructive belongings of the harmonics in inverted-fed drive system, to minimized if rms value of commutation angle [8].Two sinusoidal orthogonal envelop signals are developed from an inverse tangent method, this method have problem with amplitude deviations, dc offsets [9] and to overcome the influence of these factors go for ATO method.

Software based RDC are proving more accuracy speed position of rotor shaft angle and reduces hardware efficient demodulation of resolver outputs, in the attendance of broad distinctions of in the carrier. Based on the above observation of literature: It is mandatory to progress a speed software based RDC with high accuracy. This paper developed high accuracy software based RDC using type-II track loop algorithm with square wave excitation.

This paper organized into six sectors. In sector II Related work III describes the principle of resolver. The mathematical study and sector IV contains design methodology. Sector V contains results and discursions. In sector VI contains conclusion and future scope.

II. RELATED WORK

D.A. Khaburi and D.C Hansel man projected an offline automatic calibration method for two sinusoidal envelop signals and inverse tangent. However, these sinusoidal envelope signals are regularly disturbed by unexpected actions such as amplitude imbalances and dc offset values [4] and [7].

H.S. Patel and R.G. Hoft is planned a Pulse Width Modulation (PWM) method, intended predominantly for decrease of the injurious effects of the harmonics. It is difficult to detect the suitable sampling moments of the output signals of the resolver [8].

III. PRINCIALE OF RESOLVER

A resolver is a transducer or sensor which procedures the instant angular position of the rotating shaft to be attached it. The fundamental working principle of resolver based on the mechanical angle of their rotor into its Cartesian modules. The resolver contains primary winding is rotor and secondary feedback windings is stator. The secondary windings are relative to the Sin and Cos of rotor position (i.e.90^0 out of phase). The primary winding is excited with a voltage $V_p = E_m\sin(\omega_c t)$ then the voltages induced in the secondary windings (sine and cosine) are given by

$$V_{s13} = \alpha.E_m\sin(\omega_c t).\sin(\theta) \text{ and}$$
$$V_{s24} = \alpha.E_m\sin(\omega_c t).\cos(\theta)$$

Where ω_c is the excitation frequency

θ is position rotor angle

α is the primary to secondary winding transformer ratio.

To get conversion ratio from the primary winding to the secondary windings fluctuates with the position of resolver rotor. The basic resolver figure and the related signals are shown in Fig.1 and Fig.2 correspondingly.

Later than amplification and modulation of the resolver modulated signals results in generalized signals as: $V_s = \sin(\theta)$ and $V_c = \cos(\theta)$. The error can be extract using the resolver demodulated output signals with a suitable RDC technique.

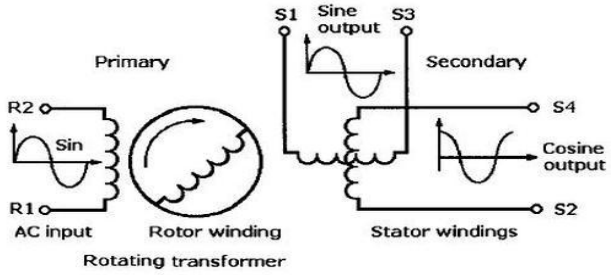

Fig.1: Basic internal structure of a Resolver

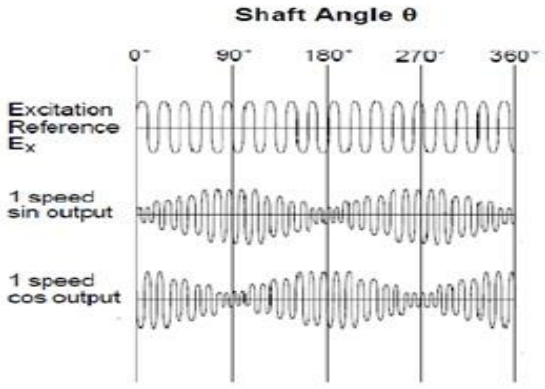

Fig. 2: Resolver excitation signal and output signals

IV. METHODOLOGY

The basic idea of the proposed type-II track loop algorithm is established from the information of digital filters, the resolver output of modulated signals are multiplied with Sin and Cos from feedback path of the speed estimation signals, conceded over a summer block and are demodulated using

synchronous detectors. while, in proposed novel type- II tracking loop algorithm, the resolver output signals are demodulated and sampled with a sample and hold by making frequency excitation of square signal, multiply with Sine and Cosine of predictable signal and are subtract to calculate the error. The proposed block diagram of software DSP based RDC using type-II track loop algorithm is shown in Fig. 3. The error signal is given to the compensator the compensator paper two different filter design ways are presented resulting designs are explain next.

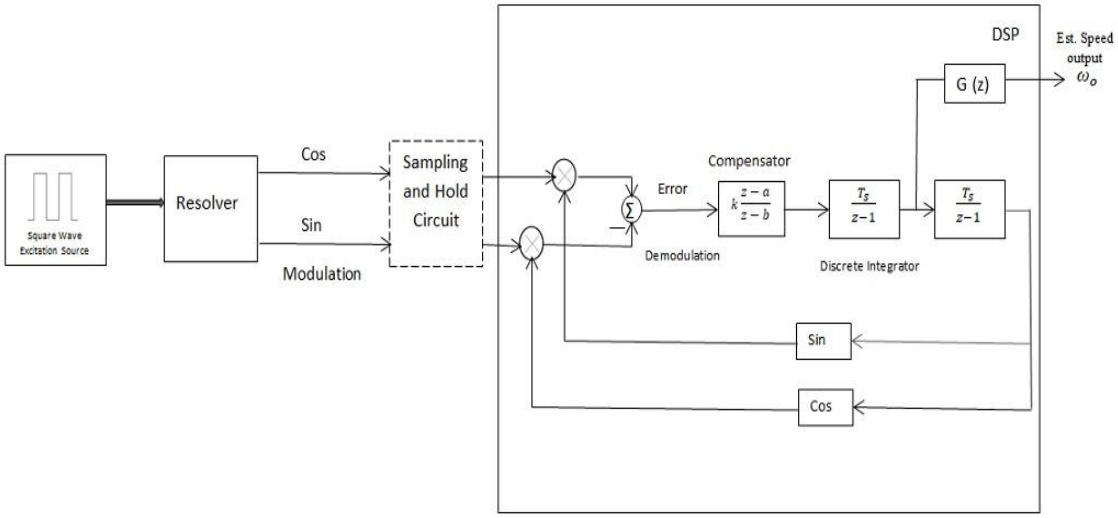

Fig.3.Bolck diagram of software DSP based RDC using type-II tracking algorithm.

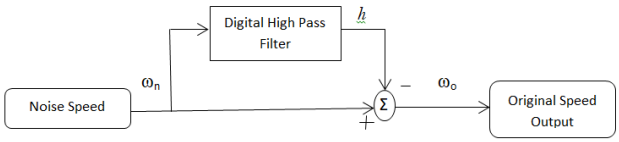

Fig.4. Digital high- pass filter model.

(1)Digital high-pass filter: The proposed digital high-pass filter is shown in Fig.4. An idea is use this filter to estimation the instant amplitude of the speed harmonics. Signals contain rapid fluctuations in their sample values are usually related with high frequency components. These high frequency components are effectively removed by a moving average filter resultant in a smoothening signal output. The simplest high pass FIR filter is obtained

$$H(Z) = \frac{1}{2}(1 - Z^{-1}) \quad (1)$$

Corresponding frequency response is given by:

$$H(e^{j\omega}) = je^{-j\omega/2}sin(\frac{\omega}{2}) \quad (2)$$

To remove the high frequency components to obtain the smooth frequency response by cascade several sections of the first order high pass filters. A high-order high pass filters of the mathematical form

$$H(z) = \frac{1}{M}\sum_{n=0}^{M-1}(-1)^n z^{-n} \quad (3)$$

It obtained by replacing z by $-z$ in the $H(z)$ of moving average filter. The noise speed output ω_n given to the digital high pass filter and unfiltered speed output signal is passed through the summer subtract h from ω_n to remove the harmonics.

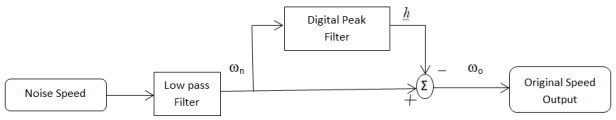

Fig.5. Digital peak filter model

(2) Digital peak filter: The digital peak filter is shown in Fig.5. An idea is develop this filter to remove the higher order harmonics of oscillatory signals, h is the instantaneous amplitude of filtered speed harmonics and ω_n before filtered speed estimation can be shown in (4) the subsequent terms in the oscillatory terms taken by the mth harmonics by compute one threshold(i.e. reference) frequency(5) for better harmonic cancellation to the respective noise speed harmonics ,the filtered speed output is given by(6) to subtract before filtered output ω_n to the instant amplitude of filtered speed harmonic h to eradicate the harmonics existing in the noise speed output response, where error e_{min} is extant due to the mismatch between $f_{ref}$of the filter and the mth harmonic frequency as a result of subsequent in the(5) exact cancelation can be only achieved digital peak filter magnitude at the frequency of harmonics to be removed.

$$\omega_n = \hat{\omega} + Asin(n\omega_n t) \quad (4)$$

$$f_{ref}=m.\omega_n$$

$$f_{ref}=m.\hat{\omega} + mAsin(n\omega_n t) \quad (5)$$

$$h=\mathrm{A}\sin(\mathrm{n}\omega_n t) + e_{min} \quad (6)$$

V. RESULTS AND DISCUSSION

The new proposed software DSP based RDC of type-II track algorithm using square wave excitation is established in MATLAB/SIMULINK and its speed authenticated performances are tested with varies speeds. The square wave excitation frequency 5kz signal is applied to resolver and time period of the excitation signals is 200µs .Fig.6.shows the square wave excitation signal, the modulated resolver output signals for a resolver speed of 150 rpm and 3000 rpm. The modulated resolver output signals are demodulated using synchronous demodulator and it is practical that the 5 kHz square wave frequency. The sampled signals of demodulated synchronous detector output signals of resolver speeds 150 rpm and 3000 rpm are shown in Fig.7. Fig.8. shows tracking speed during motor acceleration using adaptive digital filters. The performance of the new proposed software DSP based RDC system is confirmed for varies rotor speeds such as 150 rpm and 3000 rpm respectively.

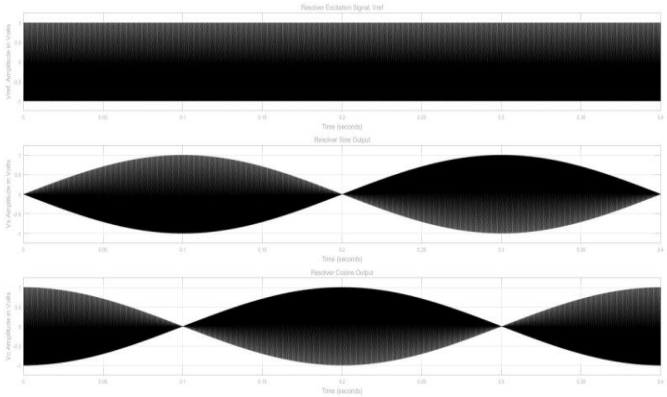

Fig.6.Squarewave, Output of resolver signals for a speed of 150 rpm

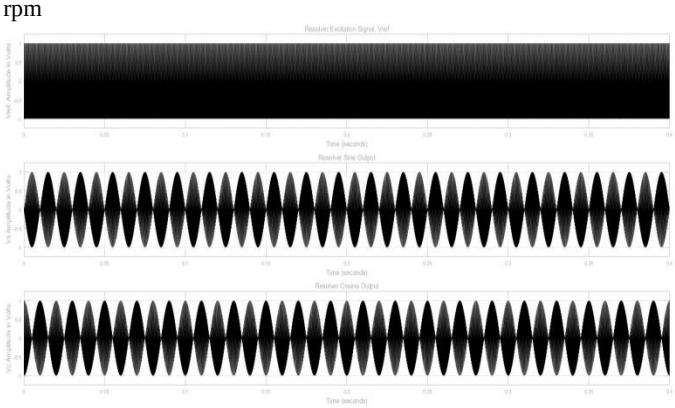

Fig.7.Square wave, Output of resolver signals for a speed of 3000 rpm

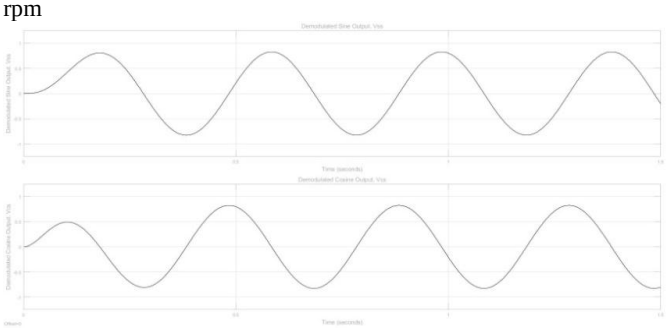

Fig.8. Sampled Signals for a speed of 150 rpm

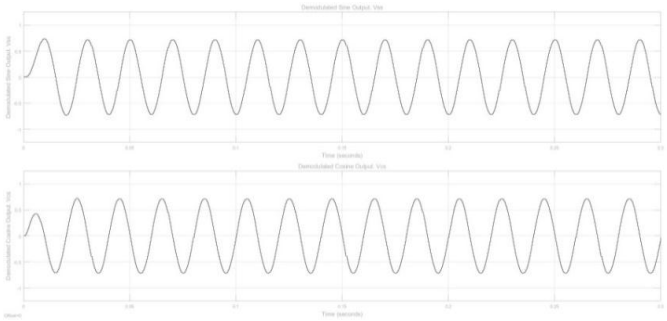

Fig.9. Sampled Signals for a speed of 3000 rpm

(1) Response with Digital high pass filter: At present, a tenth Order Digital high pass filter with pass band of 9600 Hz is intended for speed output filter G (z).

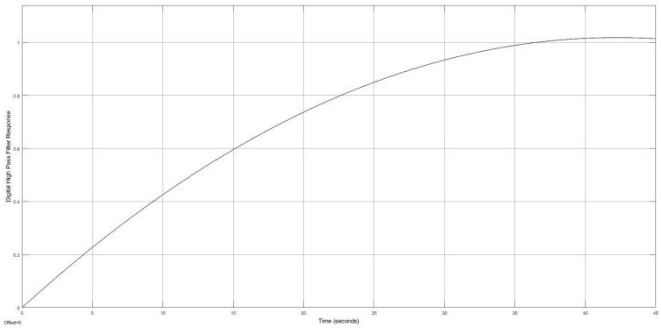

Fig.10. Speed Output of Digital high pass filter.

(2) Response with Digital peak filter: At the present, a tenth Order Digital high pass filter with f_s: 48000 Hz intended for speed output filter G (z).

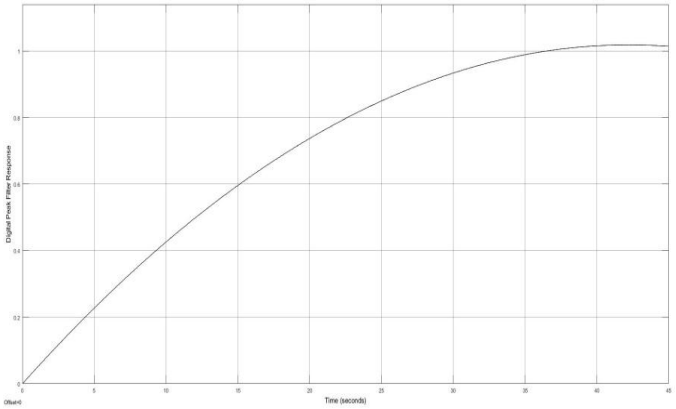

Fig. 11. Speed Output of Digital peak filter.

Parameters values for two different filters are shown in Table 1.

TABLE 1

Parameters	Digital filters	
	High pass filter	Peak filter
Structure	Direct-From FIR	Direct-Form II
Filter type	FIR Equiripple	IIR Comb
Order	10	10
Stable	Yes	Yes
Sampling frequency f_s	48000 MHz	48000 Hz
Band width	-	1200 Hz

VI .CONCLUSION AND FUTURE SCOPE

This paper presented software DSP based RDC using Adaptive digital filters with speed output of damp harmonic oscillations due to the resolver signal errors. The design of filter methods is free of any error signal or resolver constraint estimation. The two filter are implemented in this paper, the digital high pass filter is designed for signals contains rapid fluctuations in their sample values are usually associated with high frequency oscillations. These high frequency oscillations are effectively removed by moving average filter resulting in a smoothening signal output. The digital peak filter is designed for more damping performance but it requires low band width. Finally, the above adaptive digital filters are used for elimination of harmonics present in the speed output of signals. Additionally this approach is planned for fuzzy logic controller is discussed in future researches. In addition to that approaches the rotor angular position.

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