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Implementation Sobel Edge Detector on FPGA

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***Abstract*—** Recently, reconfigurable digital image processing algorithm has become growing research area in field of real-time embedded system. The edge detection algorithms are one of key area in digital image processing for object recognition or detection. These algorithms are usually implemented in software but it can be also implemented in hardware for special purpose such as high computational speed and good accuracy. This paper describes the Sobel edge detection algorithm has been designed using Hardware Description Language (HDL) and then implemented it on Field Programmable Gate Array (FPGA) devices with an emphasis on the salient features of FPGA technology. The result analysis shows that hardware implementing Sobel edge operator provide higher speed compare to software simulation. The proposed implementation uses a modified architecture which effectively reduces hardware resources. The images are transferred from PC to FPGA device using UART serial communication. The FPGA device processes the given design and result back to the PC. In PC both the results are verified.

***Keywords*—** Edge Detection, FPGA, Sobel Operator, VHDL,MATLAB.

I. INTRODUCTION

Reconfigurable edge detection method is one of the elementary parts for real-time image processing applications such as image segmentation, pattern recognition and texture feature extraction. A number of algorithms are developed for various types of image analysis. But, due to different types of their complexity and its processing speed, all the algorithms are not implementing on the hardware platform. Efficient edge detection algorithms are generally used for high speed hardware application. There are various types of edge detection technique available in image processing application. They are Prewitt, Canny, Sobel, and Roberts's algorithms which are different in terms of hardware architecture, performance and also accurateness. The Sobel edge detector is one of the simple method used for hardware realization make it easy for real-time edge detection applications [1].

Conventionally, MATLAB and C/C++ is preferred simulation tool and test for the correctness of computer vision algorithms. Today the challenging task is how to implement these computer vision algorithms to meet hard demands of the market such as real-time processing, strict power consumption and also hardware resources. The introduction of HDL such as Very High Speed Integrated Circuit with Emphasis (VHDL) [2] provided a fascinating modeling and simulation environments for fast prototyping of digital circuits and systems on FPGA devices. The FPGA technology [3] is used for digital signal and image processing applications for better accuracy and high performance in real life application. The FPGA devices provide fully re-programmable in nature with system-on-chip (SoC) environments. This architecture consists of thousands of logic gates and configurable logic blocks which make them a suitable solution for prototyping the application specific integrated circuits (ASIC) with dedicated architectures for specified digital signal applications. Hardware based image processing are much attention for electronic engineer for better performance of a given image. Hardware design techniques such as parallelism and pipelining [5] techniques can be developed on an FPGA platform, which is not found other processors like digital signal processor (DSP) or media processor. These techniques provide quicker response, flexibility and also easy upgradability. FPGA also provide optimization techniques such as they are capable of parallel I/O, which allows them to perform read (from memory) and write (to memory) simultaneously. The significant features of FPGAs such as flexibility to reprogrammable, high computing speed, low power consumption and above all low cost make them better choice in field of digital image processing. The hardware designers can be optimized and also upgraded the given architecture and simulated the system and evaluating digital circuit with timing consideration. After simulation, the generate bit streams are dumped on FPGA board. The system computational speed can be enhanced with modifies system level architecture or circuit level architecture. The only drawback of hardware simulators that it cannot support any format except binary input. So, all input and output data should be in form of

binary applicable criteria that follow.

In [4] a new technique for face detection and lip feature extraction was suggested and implemented on field programmable gate array. Design and implementation of a video image edge detection system based on FPGA was presented in [6]. In [7] an improved Canny edge detector and its realization on FPGA were presented. Implementation of FPGA based architecture of Prewitt edge detection algorithm using Verilog HDL was proposed in [8]. Image edge detection based on FPGA was described in the literature [9]. A novel FPGA-based architecture for Sobel edge detection operator was considered in [10]. In [11] performance analysis of FPGA based Sobel edge detection operator was described.

In this paper a FPGA based hardware description for implementing a real-time system for image edge detection based on Sobel operator is considered. The main advantage of Sobel operator is unaffected to noise and relatively small components required as compare to other existing operator. The method use of this operator is simple to implement and reduce the processing time. Hardware architecture of a real-time edge detection system based on VHDL is considered for high-speed processing in image edge detection.

The organization of this paper as follows: Section II describes algorithm of Sobel edge detector. Section III introduces hardware implementation and section IV reports the experimental result. Finally, the conclusion of this paper presented in section V.

II. SOBEL EDGE DETECTION ALGORITHM

The Sobel Operator [10] is a discrete differentiator operator which is particularly used image detection algorithm. This discrete differentiator operator is used to compute an approximation the gradient of image intensity function for edge detection. At each pixel of an image, the results of the Sobel operator are either the corresponding gradient vector or normal to this vector. This operator calculates the gradient of image intensity at each point, giving the direction of largest possible increase from light to dark and rate of change in that direction. The Sobel operator is based on convolve the image with a integer valued filter that is computes both horizontal and vertical direction. This operator computes the gradient using discrete differences between row and columns neighbourhood where the centre of the pixel in each row or column is weighted by two to provide smoothing. The Sobel masks in matrix form are given as

G_y		
-1	0	1
-2	0	2
-1	0	1

Figure 1. Convolution kernels in x and y direction

The two gradients computed at each pixel by convolving the above two kernels can be regarded as the x and y component of gradient vector. This vector is oriented along the direction of change normal to the direction in which the edge is runs. Gradient magnitude and direction are given by

$$G = \sqrt{(G_X^2 + G_Y^2)}$$

The approximate magnitude is as follow

$$|G| = |G_x| + |G_y|$$

The angle of the edge can be calculated gradient in the x and y direction. The edge direction is

$$\Theta = \tan^{-1}(G_y / G_x)$$

Edge strength and edge direction is equal to magnitude of the gradient and angle of the gradient respectively. It is faster to compute and simplicity calculation. But its accuracy level is low compare to any other edge detector algorithms.

III. HARDWARE REALIZATION SOBEL EDGE DETECTION ALGORITHM

The HDL language provides read and write files from a memory. VHDL is a high level language that describes any digital circuit in the form of structural description, dataflow description and behaviour description. The structural and dataflow description are concurrent in nature where behavioural description is sequentially in nature. It is relatively easy to develop a code for any VLSI engineer. The advantage of VHDL is to use any circuit, design with either in behavior domain or concurrent signal assignment and verified or simulated before the synthesis tools translate the design into real hardware. VHDL is case insensitive language. Inputs from the test benches are correctly given for a particular circuit and see the output waveform. This paper first describes Sobel edge detector methods using HDL, Verilog. Verilog only read and write ASCII characters. It does not compile bitmap or jpeg file. The basic idea of this project is to convert the input information in HDL for readable data and pass these data through the circuit described with Verilog, extract the binary results of the hardware simulation and then convert back into signal. A typical Computer Aided Design (CAD) tool provides FPGA design flow that include software tool for the tasks, such as initial design, logic synthesis, placement and routing, and programming the design into the FPGA. The tool use for FPGA implementation such as ISE from Xilinx, Modelsim from Mentor Graphics, Quartus software from Altera. Figure 2 describes the hardware model of Sobel operator.

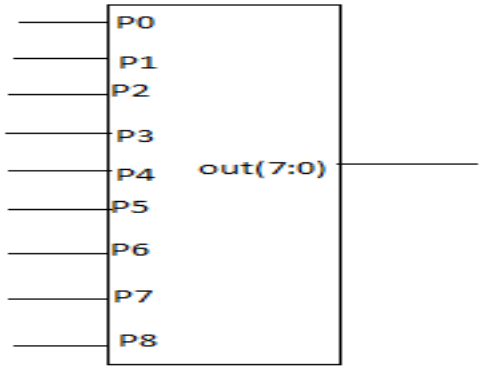

Figure 2. Sobel model in Verilog block

Here P0, P1, P2, P3, P4, P5, P6, P7 and P8 represent the eight 8-bit pixel inputs to the Sobel Module. This module consists of signed subtractions, shift registers and modulus operators. The output of the final adder block will be 11 bits (10 bits for the data as the maximum value of the adder output is 4*255 and the 11th bit as the sign bit). The output data is compared to limit the value to a maximum of 255 as the output image is also composed of 8-bit wide pixels. The limitation on the number of parallel Sobel operators that can be implemented is logic resources available in the target device.

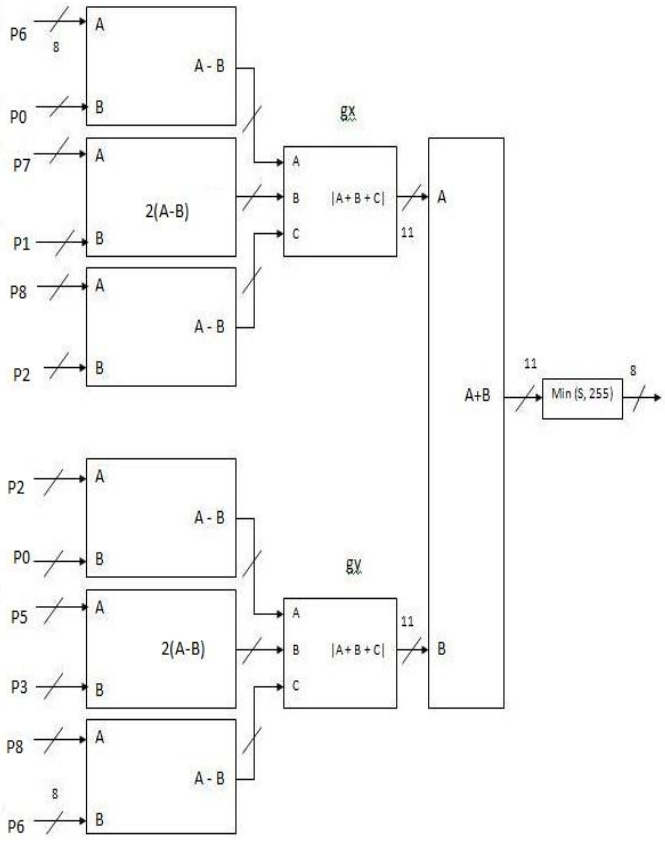

Figure 3. Architecture of Sobel model

IV. EXPERIMENTAL RESULT

The image processing algorithms discussed above were designed in ISE Design suite 14.2 and all the design algorithm is implemented on Spartan-6 FPGA based hardware. Xilinx ISE tools were used for checking synthesis, Map and Place & Route reports.

Figure 4 shows an original image and Sobel image. Here default threshold value uses for Sobel operation. The image size is considered for testing 512 x 512 pixel resolution grayscale "Lena" image. Each pixel is represented by 8 bits which means 256 intensity levels are considered during pixel processing.

Figure 4. Original image and Sobel image (right)

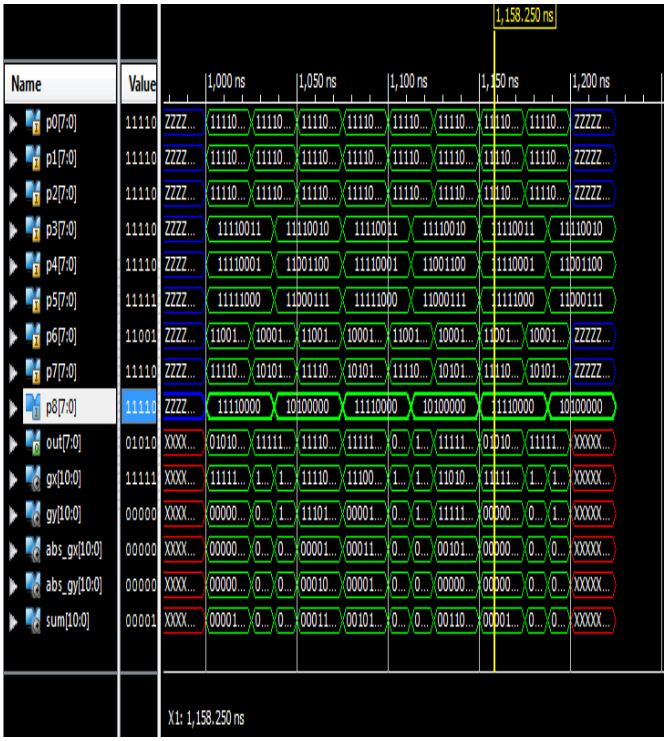

Figure 5. Hardware Simulation result of Sobel operator

Table 1 shows the comparison report of implemented algorithm. The nine inputs are considered and each input have eight bits. This table shows that slices and input-output blocks uses in this architecture.

TABLE 1. COMPARISON OF SYNTHESIS RESULT

Synthesis Parameter	[12] [13]	[15]	Proposed Architecture(Utilization)
Number Slice Registers	67	176	16(1%)
Number of Slice LUT	222	333	108(1%)
Number of used as logic	——	333	108(1%)
Number of occupied Slice	——	751(39%)	40(1%)
Number of LUT Flip Flop pairs used	222	——	108
Number of IOBs	——	80	72(33%)

Table 2 shows compilation timing report. The algorithm simulates both in software and hardware domain. Matlab and HDL provide the simulation report for software and hardware domain respectively.

TABLE 2. COMPARISON OF SIMULATION TIME

Matlab based simulation time	Hardware based simulation time
469µS	12.821nS

It is observed that hardware based simulation is faster time in processing of an image.

V. CONCLUSION

In this paper, Sobel edge detector algorithm describes on VHDL and implementing on FPGA device using Spartan-6 on XC6SLX45. This architecture requires less hardware resources compare with other edge detectors algorithms. It uses 16 Slice registers with 1% utilization. It is experimentally proved that hardware-based image processing systems are very fast compare to software based image processing. One of the major drawbacks of this hardware based image processing is inflexibility in nature. Once configured they perform their task very well. The main objective of this paper is to implement Sobel edge detector algorithm on FPGA devices with an importance on the outstanding features of FPGA technology. This system has the advantages of being simple, flexible with reasonable development cost. This method reduces the complexity of the system architecture and also reduces the computation time. The future work improvement can be done with Pipeline structure for getting higher performance. This architecture can be applicable as part of computer vision system with less number of hardware.

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