IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-6, Issue-6, June 2018 E-ISSN: 2347-2693

The impact of high-k gate dielectric on Junctionless Vertical Double Gate MOSFET

Jagdeep Rahul*
*Dept. of Electronics and Communication, Rajiv Gandhi University, Papumpare, India

**Corresponding Author: jagdeeprahul11@gmail.com.com, Tel.: +91-0360-2279005*

Available online at: www.ijcseonline.org

Accepted: 17/Jun/2018, Published: 30/Jun/2018

Abstract— In this paper, The Juctionless Double Gate Vertical MOSFET with metal gate electrode and high-k gate dielectric material (HfO_2) has been analyzed using simulation tool. The simulated results show significant improvement in its performance. In this device structure, the metal gate electrode and high-k gate dielectric material (HfO_2) are used at the place of polysilicon gate electrode and SiO_2 layer. We observed that use of metal gate electrode with SiO_2 in JLVMOS exhibits drain current (I_{dmax}) of 0.98 mA, average sub-threshold swing 67mV/dec and DIBL 61mV/V at gate voltage of 1V. When high-k gate dielectric material (HfO_2) is used with metal gate electrode in JLVMOS shows drain current (I_{dmax}) of 1.7mA, average subthreshold swing 61mV/dec and DIBL 40mV/V at gate voltage of 1V. This improvements in the performance of JLVMOS using high-k material can be utilized for high performance circuit applications.

Keywords— Junctionless Double Gate Vertical MOSFET (JLVMOS), Subthreshold swing (S.Swing), Drain Induced Barrier Lowering (DIBL), HfO_2, Workfuntion (WF).

I. INTRODUCTION

The shrinking of MOSFET beyond 50 nm technology node requires innovative device structure to overcome the short channel effects. In conventional MOSFET structure, formation of P-N junction between source to channel and drain to channel is become the fabrication challenge beyond 32 nm CMOS technology [1, 2]. The short channel effects start degrading the performance of the device when channel length is reduced to the order of channel depth. The issues most often created are due to the short channel effects are subthreshold slope, DIBL, Sub threshold leakage current and hot carrier effect. In Junction-less double gate vertical MOSFET, Vertical MOSFET devices represent a new category. In this structure the planar arrangement of the source, gate and drain is turned through 90 degree so that they are positioned on top of each other and the electrons flow in perpendicular to the surface. In junctionless devices substrate is lightly dopped (n-type: N and p-type: P) as compare to the source and drain [3]. The doping level in junction-less double gate vertical MOSFET is same as the junctionless double gate planner MOSFET, source, channel, and drain of JLVMOS is identical (n-type: N+-N+-N+ and p-type: P+-P+-P+) and does not form any P-N junctions between the source/drain and channel. For N-type junctionless device requires a gate material with a high work function equal to P+ polycrystalline silicon or platinum to achieve a suitable threshold voltage [4].

The advantages of JLVMOS are better controlling capability of gate over channel region and reduced short channel effects. The fabrication process of vertical MOSFET doesn't require advanced lithography to achieve the short channel length specially in nano-meter regime. The fabrication process of junctionless devices is very simple as compare to conventional MOSFET, since there is no doping concentration gradient required for source and drain during the time of fabrication of the device. It also saves a lot of thermal cost in fabrication process [5].

Demand of industries is to integrate more functionality, higher performance and high package density of transistor on a single chip. Scaling of device includes the channel length, gate dielectric thickness and drain voltage to maintain the constant electric field inside the channel. Many high-k materials like Zirconium dioxide, Hafnium dioxide, etc. have potential to replace the Silicon dioxide as gate dielectric material, where below 2nm oxide thickness required. The selection of high-k material depends on permittivity, band gap, interference with silicon, thermodynamic stability and compatibility with fabrication process. The properties of Hafnium dioxide (HfO_2) is found suitable for JLVMOS at the place of SiO_2 layer [6]-[8].

In this paper, first SiO2 layer with tunable work function metal gate electrode and secondly HfO_2 with tunable work function metal gate electrode ranging from 5.0 eV to 4.8 eV

has been investigated in JLVMOS for performance evaluation.

II. DEVICE STRUCTURE

The structure of JLVMOS consist double gate, drain, source, channel length, oxide thickness (T_{ox}), body thickness(T_{sc}) and channel dimensions of the device explicitly shown in the figure1. The depletion effect arises due to polysilicon gate electrode, when gate voltage is applied; created electric field keeps away the carriers and form depletion layer in polysilicon. In the absence of charge carriers non mobile dopant atom becomes ionized. This polysilicon depletion layer reduces the electric field at the surface of the channel. The reduced electric field degrade the overall performance of the device. The use of metal gate electrode at the place of polysilicon gate electrode eliminates the carrier depletion layer. The threshold voltage may be controlled by tuning work function equal or near to value of polysilicon gate [10, 11]. The threshold voltage is the difference of work function of semiconductor and material used in gate electrode. The metal gate electrode of work function of 5.27eV may replace the P-doped polysilicon of N-type junctionless MOSFET.

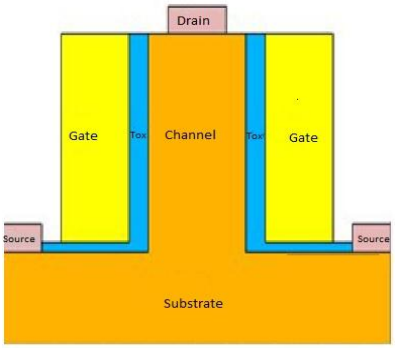

Fig1: 2D Structure of Junctionless vertical double gate MOSFET

Notably, junction-less MOSFETs demonstrate substantially lower gate capacitances in saturation region and a slower degradation of transconductance with gate overdrive voltage. With its unique advantage is the elimination of the source/drain junctions, junction-less MOSFETs could be a promising candidate for future sub-10 nm technologies where a 3-D gate structure is most likely required.

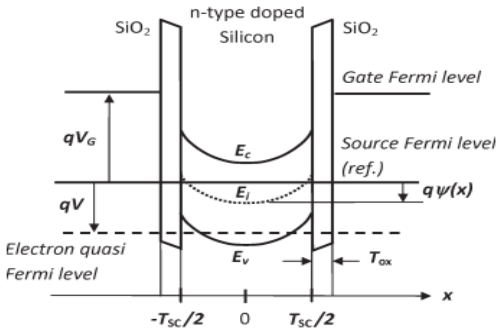

Fig2: Sketch of the energy diagram of junctionless MOSFET [9]

The dielectric constant of high-k materials is subsequently higher than silicon dioxide (k_{ox}), which results smaller equivalent oxide thickness (EOT) than SiO_2 but physical thickness of high-k material (HfO_2) is greater than the silicon dioxide [11].

$$EOT = \frac{k_{ox}}{k} \times t_{Physical}$$

The use of high-k material having different dielectric constant at the place of silicon dioxide is not easy in fabrication process. The dielectric constant approx 25 of HfO_2 has been used at the place of silicon dioxide with metal gate electrode in JLVMOS. The HfO_2 with physical thickness of 3nm with calculated EOT is about 0.5nm is used at the place of silicon dioxide, which improves the controlling capability of gate over channel. We have assumed high doping concentration at channel ($1x10e^{-19}cm^{-3}$) for small threshold variation, the channel thickness of 10nm, oxide thickness (HfO_2) of 3nm. The device has been simulated for different work function of metal gate electrode ranging from 4.8eV to 5.2eV. The metal gate technology has potential to replace conventional polysilicon gate technology for junctionless devices for better performance[13 14].

III. RESULTS AND DISCUSSION

The transfer and drain characteristics of JLVMOS with metal gate electrode and silicon dioxide are shown in figure 3 and 4 respectively. The junctionless VMOS shows 0.98mA drain current with metal gate electrode having workfunction of 5.1eV and that is higher than polysilicon gate electrode. The drain characteristics of JLVMOS have been obtained at the gate voltage of 1.0V. The workfunction of metal gate electrode has ability to change the threshold voltage of the device. The decrease in the workfunction results early accumulation of charge carriers below the gate surface without adding any extra doping the substrate.

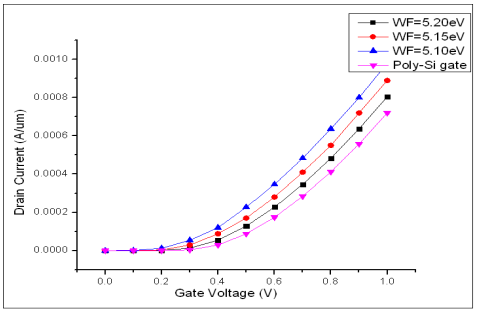

Fig.3: Transfer Characteristics of JLVMOS.

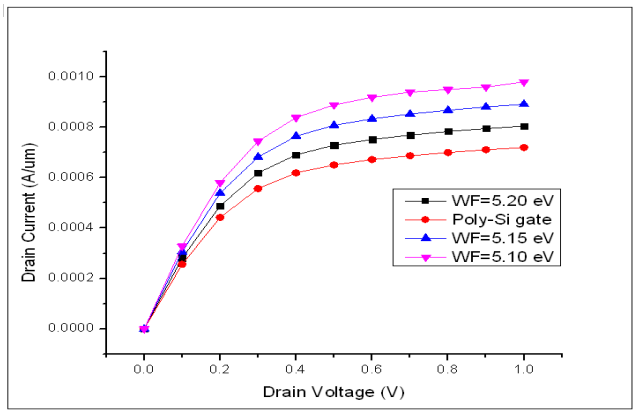

Fig.4: Drain Characteristics of JLVMOS at different gate voltage.

The device structure with high work function (5.2eV) has lower DIBL, subtrheshold swing, low leakage and high threshold voltage as compare to device having gate electrode with workfunction (5.10eV). The comparison of metal gate electrode with different workfunction and polysilicon gate electrode is shown in table1. The advantages of metal gate electrode are no depletion layer, no boron penetration and sheet resistance is very low in comparison to polysilicon gate electrode.

Device	I_{dmax} (A/um)	S.Swing (mV/decade)	DIBL (mV/V)
JLVMOS (Poly-Si gate)	7.2×10^{-4}	63.74	44.29
JLVMOS + Metal Gate(WF)=5.20 eV	8.05×10^{-4}	64.94	52.3
JLVMOS + Metal Gate(WF)=5.15 eV	8.92×10^{-4}	65.95	58.7
JLVMOS + Metal Gate(WF)=5.10 eV	9.81×10^{-4}	67.10	61.4

Table1: Comparison table of JLVMOS with metal gate electrode and Polysilicon

When high-k material (HfO_2) is used with metal gate electrode in JLVMOS produced better results like DIBL, subthreshold swing, higher threshold voltage and low leakage current as compare to metal gate electrode shown in Table2. The device using metal gate electrode with workfunction 4.80eV and HfO_2 produces higher value of drain current compare to others but also having higher leakage current. The short channel effects like DIBL and S. Swing at work function of 4.8eV are 40mV/V and 61 mV/dec respectively. The use of HfO_2 in device increases interface charge density at the surface and degrade the mobility of charge carrier due to that gate capacitance gets increased.

Device	I_{dmax} (A/um)	DIBL (mV/V)	S.Swing (mV/dec)
Poly Gate +SiO_2	7.2×10^{-4}	44	63
Metal gate (WF =5.0eV) +HfO_2	0.001070	35	60
Metal gate (WF=4.9eV) +HfO_2	0.001429	38	60
Metal gate (WF=4.8eV) +HfO_2	0.001772	40	61

Table1: Comparison table of JLVMOS with metal gate electrode with HfO_2 and polysilicon gate electrode.

The use of metal gate electrode with high-k gate dielectric (HfO_2) in junctionless devices produces better results in terms of drain current, leakage current and also highly immune to the short channel effects.

IV. CONCLUSION

The use of metal gate electrode with HfO_2 produces better device characteristics with an average subthreshold swing and DIBL. The drain current of junctionless device can be increased by tuning the work function of the metal gate electrode without adding any extra dopent to the channel. Any extra doping in the channel degrades the mobility of charge carrier at high temperature. The metal gate with workfunction 4.8eV produced 150% more drain current as compare to the polysilicon gate and subthreshold swing, DIBL are still in acceptable range.

V. REFERENCES

[1] Y. Taur, "CMOS design near the limit of scaling," *IBM J. Res. Develop.*, pp. 213– 222, 2002.
[2] Ismail, razak M. A et al., "Design and simulation analysis of Nanoscale vertical MOSFET Technology" SCOReD, pp. 215-218, 2009.

[3] C.-W. Lee,et al., "Performance estimation of junctionless multigate transistors," Solid-State Electronics, vol. 54, pp. 97-103, , 2010.
[4] Xin Qian, Yinglin Yang, et al., "Evaluation of DC and AC performance of junctionless MOSFETs in the presence of variability" IEEE conference on ICICDT, 31 May 2011.
[5] Jagdeep Rahul, Shekhar Yadav, Anurag Srivastava, et al., "Performance Evaluation of Junctionless Vertical Double Gate MOSFET," *IEEE conference on* ICDCS, pp. 440 – 442, 15-16 March 2012.
[6] Shekhar Yadav, Jagdeep Rahul, Anurag Srivastava , et al., "TCAD Assessment of Nonconventional Dual Insulator Double Gate MOSFET ," *IEEE conference on* ICDCS, pp. 462 – 465, 15-16 March 2012.
[7] B. Cheng, et al., "The impact of high-k gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, pp.1537-1544, July 1999.
[8] G. Ribes et al., "*Review on High-k Dielectrics Reliability Issues, IEEE Transactions on Device and Materials Reliability*, Vol. 5, no. 1, pp. 5–19, 2005.
[9] Duarte, J.P. Sung-Jin Choi, et al., "Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors," *IEEE Electron Device Lett.* vol. 32, no. 6, pp.704-704, 2011.
[10] S. M. Nawaz, A. Mallik, "Effects of device scaling on the performance of junctionless finfets due to gate-metal work function variability and random dopant fluctuations", IEEE Electron Device Lett, vol. 37, no. 8, pp. 958-961, Aug. 2016.
[11] Y. Li, C. H. Hwang, T. Y. Li, M. H. Han, "Process-variation effect metal-gate work-function fluctuation and random-dopant fluctuation in emerging CMOS technologies", *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437-447, Feb. 2010.
[12] V. Narendar, R. A. Mishra, " Analytical modeling and simulation of multigate FinFET devices and the impact of high- k dielectrics on short channel effects (SCEs) ", *Superlattices Microstruct.*, vol. 85, pp. 357-369, Sep. 2015.
[13] Basab Das "GaN channel Nanoscale MOSFET with Silicon Source and Drain and Silicon Germanium Bulk" International Journal of Computer Sciences and Engineering, Vol.-4(7),pp-140-143, Dec 2016.
[14] Karishma Bajaj et al"CMOS Technology Vs Carbon Nano Scale FET's " International Journal of Computer Science Engineering, Vol. 5 No.05, pp-277-280, Sep 2016.

Author Profile

Mr. Jagdeep Rahul pursed Bachelor of Technology from Bundelkhand University, India in 2009 and Master of Technology from ABV-IIITM in year 2012. He is currently pursuing Ph.D. and currently working as Assistant Professor in Department of Electronic and Communication, Rajiv Gandhi University, India since 2015.

