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FPGA Realization of PWM using HDL

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***Abstract*—** Pulse Width Modulation (PWM) is an essential technique for many electrical applications. It is mainly used for controlling DC power to an electrical device. It can be used in applications where its duty cycle is used to convey information over a communication channel. Though many software designs and hardware models are available for PWM, FPGA modules are reliable in terms of speed and complexity. Hardware optimization is possible in FPGAs. Hence work is focused to realize the PWM on FPGA. In this paper hardware model of PWM using HDL is presented. This model is designed using VHDL and implemented on VIRTEX FPGA Device. Simulation is carried using Xilinx ISE. The RTL Design is synthesized using Xilinx XST and the generated bit stream file is implemented on Virtex FPGA board.

***Keywords*—**PWM, RTL, VHDL, FPGA

I. INTRODUCTION

PWM is fundamental concept for control in power systems. Ideal PWM signal with zero delay of rise and fall times provide best way of driving modern semiconductor power electronic devices. Precision and protection are of important parameters in DC motor speed control and it can be achieved by using PWM. The width [1] of the pulse controls the sped of motor shaft by regulating its energy. Based on the PWM concept, if duty cycle is changed as sinusoid, a sinusoidal voltage will be generated at the output. Some PWM methods are aimed at [12][13] making better use of the DC bus voltage and thus increasing modulation index. The pulse-width modulator is also an integral part of the feedback control loop and needs to be properly modelled for control design.

The important property of PWM is that it [2][3] has low power loss in switching devices and high frequency that affects the device which uses power. Based on the property of PWM the following technique is adopted to implement PWM on a digital device.

PWM uses rectangular pulses where width is modulated by carrier signal resulting in the variation of average value of the waveform. Figure 1 demonstrates the PWM concept where the width of the modulate signal is maximum when the carrier signal amplitude is maximum. Here the carrier signal is arbitrary but for the[14][15] realization a sine signal is used.

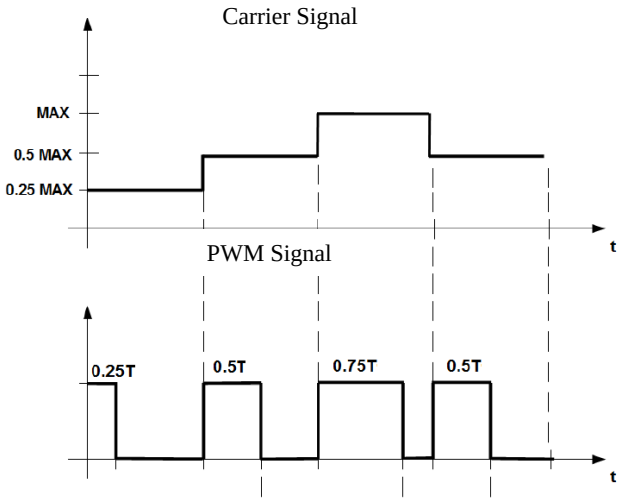

Figure 1. PWM Signal Representation

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can [4] be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.

FPGA based devices have less delay, flexible in design, reduction in hardware and more [5] important it is reprogrammable. Due to their programmable nature, FPGAs are an ideal fit for many different markets.

The conceptual model of the PWM is implemented using Virtex 5 XC5VLX50T FPGA board. In Section 2, architecture of the modulator is elaborated and details of blocks are explained in sections 3, 4, 5. Implementation of the module is placed as section 6 and the evaluated results of the modulator design with the required information of screenshots are placed in section 7. And at last the Conclusion and future scope are covered in final sections.

II. ARCHITECURE

The architecture of the PWM Modulator is shown in fig.2 It consists of Digital Sine Generator, Frequency trigger, and FSM Module.

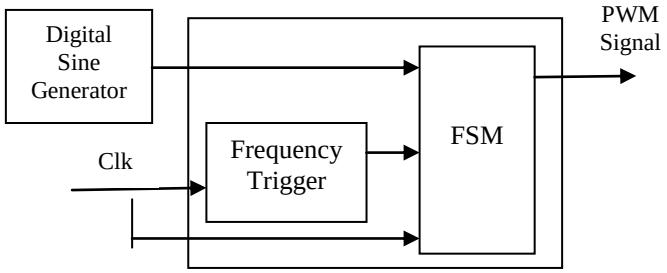

Figure 2. Block diagram for PWM Modulator

Digital Sine generator is used to generate digital values of analog sine wave. Frequency trigger is used to generate analog sine wave and is used in digital sine generator. The same module is used again to generate higher frequency so as to get proper PWM signal. FSM is [6] finite state machine which is the key module for generating variable pulse width.

Initially analog sine wave is generated and its digital representation is stored using a clock signal. Depending up on the sine values the FSM will modulate the width of the pulse.

VHDL programs are written for digital sine generator, frequency trigger and FSM. Finally a top level module which is a PWM module is written comprising the above modules.

III. DIGITAL SINE GENEARTOR

This module will generate a digital representation of an analog (sine) signal with desired frequency. It will use the counter values as addresses to fetch the next value of the sine wave from the ROM. In this paper a [7] VHDL package with a parametrized sine signal is designed. To represent sine wave 256 unsigned amplitude values are used for one sine period that will be stored into an ROM array. VHDL package is a way of grouping related declarations that serve a common purpose. Each VHDL package contains package declaration and package body.

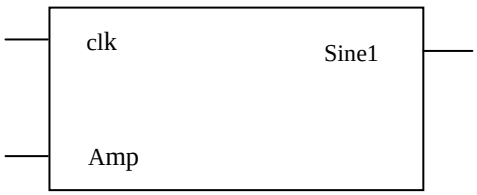

Figure 3. Block diagram for Digital Sine Generator

```
process
begin
wait until rising_edge(clk_in);
amp1 <= conv_integer(amp_l);
std_logic_vector type……..
…….
……
sine1 <= conv_std_logic_vector(sin1_c, width_g);
end process;
```

IV. FREQUENCY TRIGGER

This module is used in digital sine generator and used separately before FSM to generate PWM signal. The [8] main purpose of this module is to generate sine signal of desired frequency.

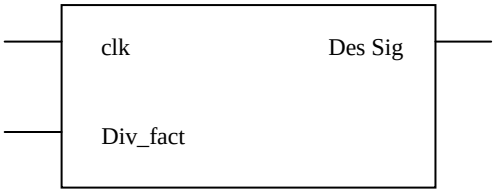

Figure 4. Block diagram for Frequency Trigger

Div_fact is used to choose the desired frequency of sine signal.

```
…….
……..
if (sw0 = '0') then
if (freq_cnt_s >= div_factor_freqlow - 1) then
freq_trig <= '1';
freq_cnt_s <= 0; -- reset
end if;
else
   if (freq_cnt_s >= div_factor_freqhigh - 1) then
……..
…….
```

The same frequency trigger is used before FSM to generate higher frequencies so as to regulate the PWM output.

V. FSM

FSM module will generate the PWM signal. It will generate the PWM signal with correct duty cycle for each period

based on the current amplitude value of digital sine signal that is stored in the ROM. FSMs are [9][10] important to specify sequential machines with states, inputs and outputs. FMS can be Mealy or Moore machine. Design can be carried out easily if the system is defined in terms of FSM.

State diagram of the FSM is shown on the Figure 5.

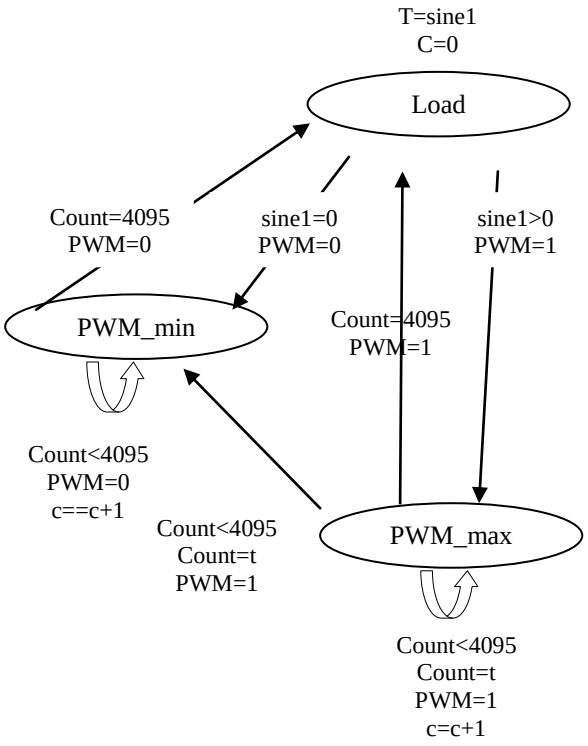

Figure 5. FSM for PWM

VI. IMPLEMENTATION

The entire system is realized using Xilinx tool. Initially VHDL programs are written for counter, frequency trigger, sine wave and top level module for PWM. Then constraints file [2] with pinout and area constraints and timing constraints are added to the top module file. All the files are simulated and finally top module is verified for its functionality.

Simulated top module file along with constraints file are synthesized for generating gate level netlist. The RTL schematic and Technology schematic files are used to interpret the design. Then the synthesized file is translated, mapped and routed according to the device. At each step of synthesis and [2][11] implementation, reports are generated to describe the hardware structure of the FPGA device. Later bit stream file is generated and is dumped into the FPGA. The functionality of the module in FPGA can be verified by using chipscope pro. If the target device is changed then entire process is to be repeated from synthesis. Synthesis is a device specified process. It generates reports based on the target used.

VII. RESULTS

The Design entry of PWM is done using VHDl and simulated using Xilinx ISE. The design is synthesized using Xilinx 10.1 synthesis tool and implemented on Virtex XC5VLX50T FPGA Board.

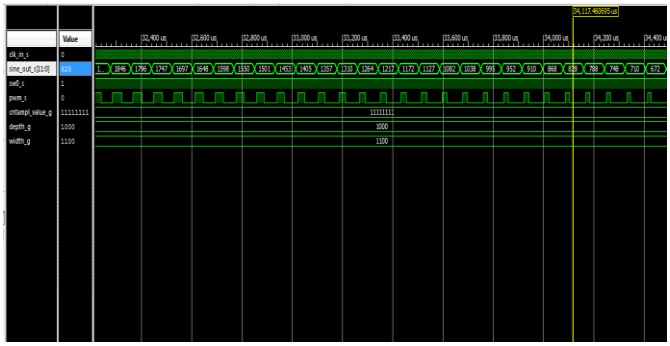

Figure 6. Simulation Waveform of PWM

Fig 6 shows the simulation waveform of proposed multiplier. In the Figure the width of the pulse changes as the values of sine_out varies. As the value is more the on period of pulse is more and on period decreases as value of sine_out decreases.

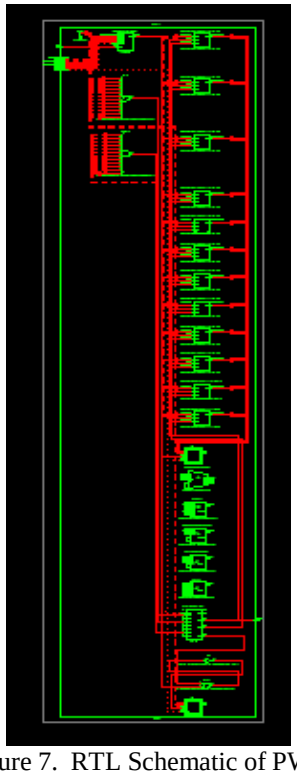

Figure 7. RTL Schematic of PWM

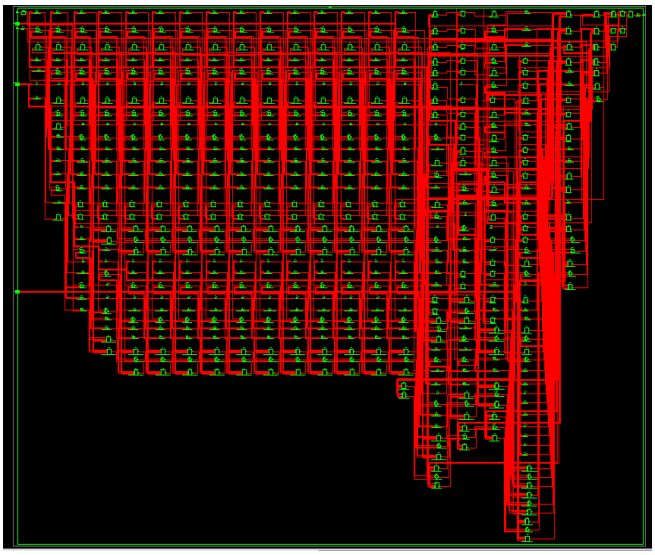

Figure 8. Technology Schematic of PWM

Selected Device: 5vlx50t-3ff1136

Table 1 Synthesis Report

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	59	28800	0%
Number of Slice LUTs	216	28800	0%
Number with an unused Flip Flop	216	28800	0%
Number with an unused LUT	167	226	73%
Number of fully used LUT-FF pairs	10	226	4%
Number of unique control sets	49	226	21%
Number of bonded IOBs	79	480	16%

Table 2 Timing Report

Parameter	Value
Minimum Period	3.787ns
Maximum frequency	264.082Mhz
Minimum input arrival time before clock	4.879ns
Maximum output required time after clock	3.359ns

Table 3 Power Report

Parameter	Value in mw
Clocks	3.25
Logic	0.11
Signals	0.21
IOs	0.46
Quiescent	560.49
Total	564.52

VIII. CONCLUSION

In this paper a hardware realization of PWM modulator is presented. PWM modulator having more importance in power electronics and thus it needs more accuracy and flexibility in the implementation. FPGA provides better way of realizing the systems by writing the code in VHDL and realizing using convenient tools. In this paper a VHDL code is written for PWM and is realized on a Virtex FPGA kit. Results show that accurate PWM pulses can be generated using this method.

IX. FUTURE SCOPE

The same design can be implemented on SOC devices which are far sophisticated than present used FPGA. Some of the devices are Zync devices which have a microcontroller and FPGA for getting high performance. But the tool and method of operation is changed. For those devices other than HDLs also can be used.

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