IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-6, Issue-11, Nov 2018 E-ISSN: 2347-2693

Power Factor Improvement of Buck-Boost AC-DC Converter using Pulse Width Modulation Strategy

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Available online at: www.ijcseonline.org

Accepted: 21/Nov/2018, Published: 30/Nov/2018

***Abstract*—** In power electronics converters applications, the input current to the converter contains a harmonic current which leads to the low power factor. The paper attempts to develop a pulse width modulation (PWM) strategy with a view to improve the input power factor of a buck boost ac-dc converter. The difficulties in the choice of corner frequencies for filter circuits emphasize a resurgent focus on the boundaries of PWM approaches and arbitrate to traverse a fresh direction for enjoying its benefits. The theory relates to the use of two level saw tooth carrier to arrive at the appropriate pulses for both the switches. The philosophy manifests to reshape the input current waveform in an effort to phase align the same with the supply voltage. The scope travels to examine the performance of the methodology using MATLAB based simulation and involve the use of an experimental prototype to validate the results and there from establish its suitability for use in the practical world.

***Keywords*—** Input power factor, Buck Boost converter, PWM, Microcontroller.

I. INTRODUCTION

Traditionally AC-DC conversion is accomplished through the use of full bridge rectifier and a capacitor filter at the output to absorb the pulsations and thereby reduce the ripple in the output voltage. However this conventional technique does not augur for the true value of input power factor to be close to unity. Low power factor reduces the power available from grid and may end up de-rating the utility system.

AC-DC converters are electronic devices used wherever a change in fixed ac to fixed dc from one voltage level to another is required. The most commonly used ac-dc Converter, namely the simple diode bridge rectifier however produces only a pulsating dc output. AC-DC converters become interesting in low power applications since they present lower cost and complexity in comparison to classical two stage approach.

AC/DC power converters are extensively used in various applications like power supplies, dc motor drives, front- end converters in adjustable-speed ac drives, HVDC transmission, SMPS, fluorescent lights (with electronic ballasts), utility interface with non-conventional energy sources, in process technology like welding, power supplies for telecommunication systems, aerospace and military environment.

Switch mode Power Factor Corrected (PFC) ac-dc converters with high efficiency and power density are being used as front end rectifiers for a variety of applications. The converters are either buck or boost type topologies [1]. The buck type topology provides variable output dc voltage, which is much lower than the input voltage amplitude. However when the instantaneous input voltage is below the output dc voltage, the current drops to zero that results in significant increase in input current THD. Even with input filters the buck converters provide only limited improvement in input current quality. These ac-dc converters provide stable dc voltage at the output with high input power factor. This capability makes PFC converters an extremely attractive choice for offline power supplies and other ac-dc power conversion applications because of increasing concerns about power quality and to meet the guidelines of various power quality regulations and standards. Since these converters cater to the unique requirements of a large number of applications, several control strategies and topologies need to be evaluated and developed to meet the specifications of the target application.

An ideal power factor corrector is required to act as a resistor emulator on the supply side and simultaneously maintain regulated output voltage. There is a need to device better alternatives and envisage a methodology to improve the input power factor [2-3]. The immediate claims are lowering of the VAR requirements, lower

stress on the power switches.

A host of control strategies for power factor correction in ac-dc converter have been studied and their performance compared [4]. An average current control technique has been

applied to the cascaded buck-boost converter to improve the input power factor [5]. A new ac-dc power electronic converter topology has been suggested for efficient and optimum energy harvesting from low- voltage micro generators [6].

A bridgeless power factor correction boost converter has been proposed [7] to address power factor improvement and reduce the harmonic content in input line currents. An ac–dc single-stage high-power universal PFC has been realized through an ac input full-bridge, pulse-width modulated converter [8].

Though extensive efforts continue in this perspective [9-12], still considerable focus is required to cleave out refinements in the formulations and ensure improvements in the performance. It is therefore proposed to design a pulse width modulation (PWM) strategy suitable for the two switches in the Buck-Boost topology to pull out an enhanced input power factor and regulated load voltage.

II. PROBLEM FORMULATION

The primary directive extends to translate a PWM scheme in order that it offers a facility to shape the input current waveform to a sinusoidal fashion and provide an impetus to correct the input power factor. The exercise incites to evaluate its performance through both simulation and hardware implementation over a range of operating loads.

III. PROPOSED METHODOLOGY

The theory echoes to formulate a wave shaping mechanism through the process of PWM switching and engrave a sequence to bring the input current vector along the voltage waveform.

The power module seen in Fig.1 operates either as a buck or boost converter depending upon the input output conditions. The switch S1 is always on and S2 is operated for the converter to serve as a boost converter. On the other hand when it works as buck converter, the switch S2 is off and S1 is operated. It throws open lower stresses on the switches in view of the fact that they are operated only twice in each mode of operation.

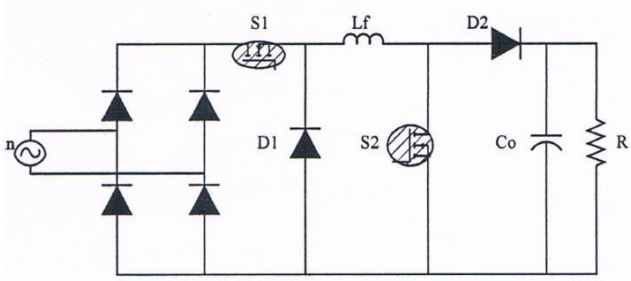

Fig.1 Buck-Boost Converter

The buck and boost modes carry with them two sequences of operation. The Figs. 2(a) and 2(b) display the sequence 1 and 2 of the boost mode. With the inductor current and capacitor voltage as state variables, the state equations for sequence 1 are derived as in Eqns. 1 and 2.

$$\frac{di_L}{dt} = \frac{1}{L}|u_i| \tag{1}$$

$$\frac{dV_c}{dt} = \frac{1}{RC}V_c \tag{2}$$

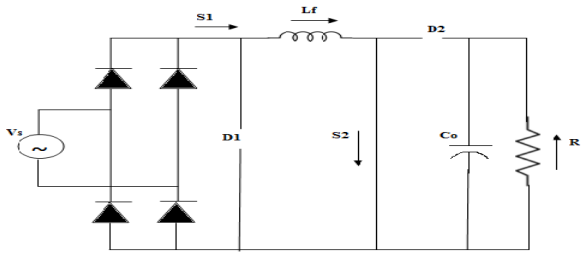

Fig. 2a Sequence 1(boost), switch S_2 is ON

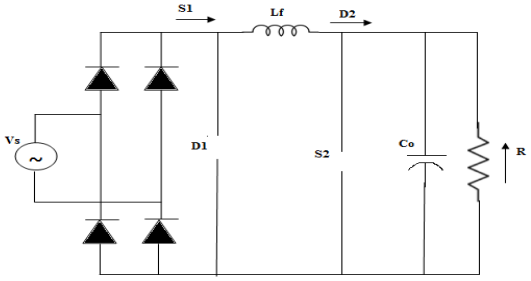

Fig. 2b Sequence 2(boost), switch S_2 is OFF

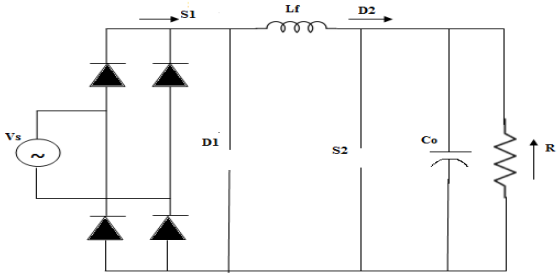

Fig. 2c Sequence 3(buck), switch S_1 is ON

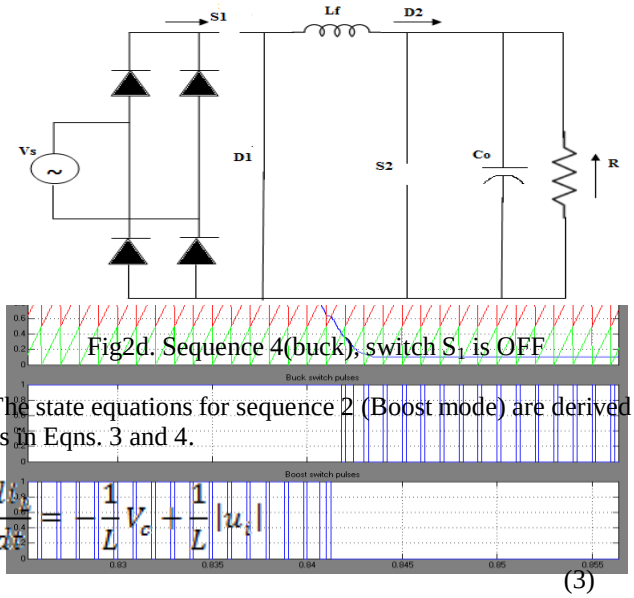

Fig2d. Sequence 4(buck), switch S_1 is OFF

The state equations for sequence 2 (Boost mode) are derived as in Eqns. 3 and 4.

$$\frac{di_L}{dt} = -\frac{1}{L}V_c + \frac{1}{L}|u_i| \quad (3)$$

$$\frac{dV_c}{dt} = \frac{1}{C}i_L - \frac{1}{RC}V_c \quad (4)$$

Similarly the buck mode follows two sequence of operation 3 and 4 seen in Figs. 2c and 2d depending upon the state of switch S1. The state equations can be derived as in Eqn. 5 and 6.

$$\frac{di_L}{dt} = -\frac{1}{L}V_c + \frac{1}{L}|u_i| \quad (5)$$

$$\frac{dV_c}{dt} = \frac{1}{C}i_L - \frac{1}{RC}V_c \quad (6)$$

The state equations in sequence 4 as in Eqns.7 and 8.

$$\frac{di_L}{dt} = -\frac{V_c}{L} \quad (7)$$

$$\frac{dV_c}{dt} = \frac{1}{C}i_L - \frac{V_c}{RC} \quad (8)$$

IV. CONTROL ALGORITHM

The methodology echoes to design the PWM algorithm with a primary focus to generate the PWM pulses for the two power switches. It enforces the requirements of regulating the load voltage and improving input power factor.

The input ac voltage is converted to the dc voltage through the use of diode bridge rectifier. The variable dc voltage acquired from is given to the load from where the error between the load voltage and actual voltage is calculated.

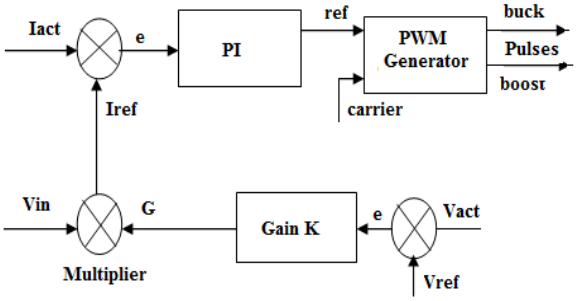

Fig.3 Control Algorithm

The voltage error is multiplied with constant gain K to determine the equivalent conductance. The equivalent conductance is compared with the input voltage to generate the reference current. The current reference is compared with the actual current to estimate how far the actual current is away from the sinusoidal reference voltage. The error is corrected through the PI controller as a part of wave shaping mechanism to produce the reference wave for the PWM pulses. The two level saw tooth carrier along with reference produces PWM pulses for the two power devices.

V. SIMULATION RESULTS

The procedure travels to investigate the methodology on a MATLAB platform. The specifications reiterate to support 230V, 3.5kW RL load. The Fig. 4 exhibits the PWM pulses of the concurrent operation of both boost and buck modes. The dc output voltage for two distinct buck and boost set points shown in Figs. 5 and 6 respectively further elaborate the regulating ability in both modes. The result of regulatory disturbance projected in Fig. 7 explains the fortitude of the strategy to remain regulated at their respective operating points even when it is subjected to a sudden 10% change in load. The input voltage and current waveforms seen in Figs. 8 and 9 refer to the open and closed loop modes and bring out the ability of the control scheme to improve the input power factor at the 1kW operating point.

Fig. 4 PWM output waveforms

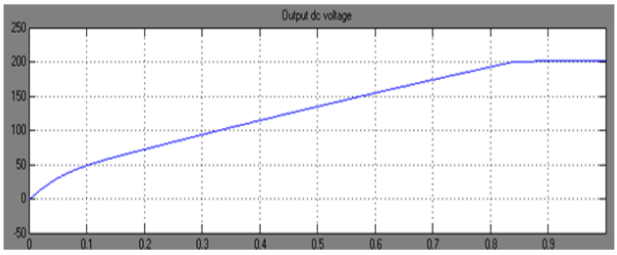

Fig 5. Output dc voltage for a set point of 200 volts

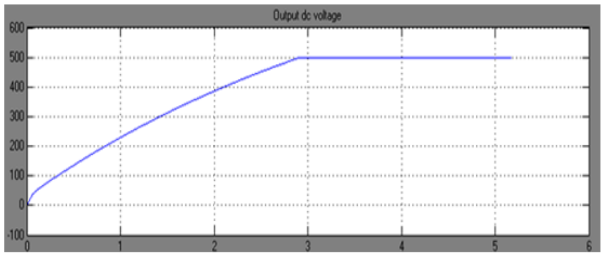

Fig. 6. Output dc voltage for a set point of 500 volts

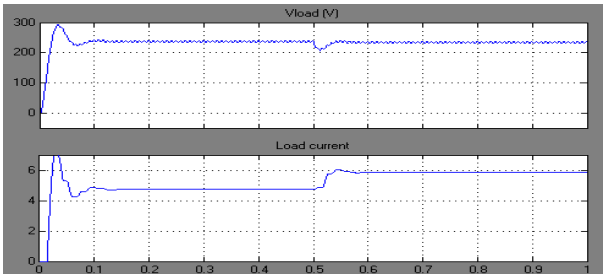

Fig. 7 Transient voltage and current waveforms

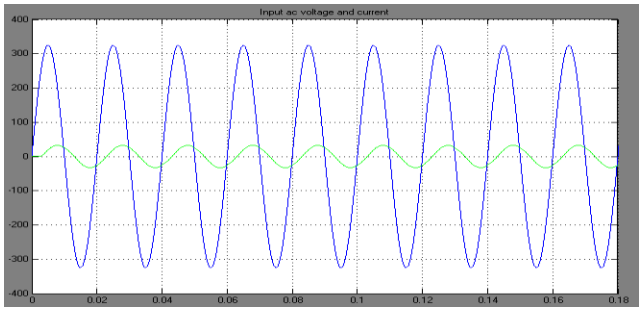

Fig. 8. Input ac voltage and current waveform in open loop

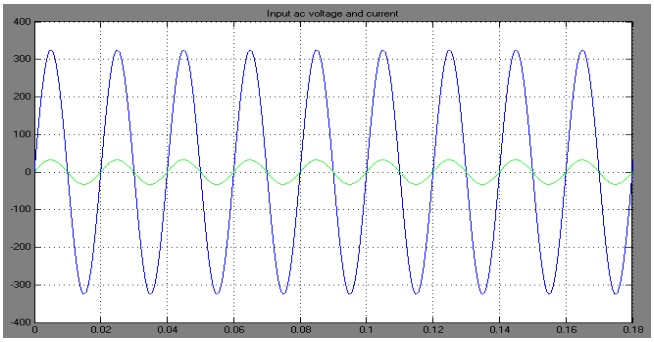

Fig 9. Input ac voltage and current waveform in closed loop

VI. HARDWARE IMPLEMENTATION

The task extends to validate the performance using a prototype of the buck-boost converter. It etches the role of P89C51RD2 microcontroller to function as a PI controller and also serves to generate PWM pulses for the power switches in the converter.

The feedback arrangement is built through a signal conditioning circuit and an associated ADC. The micro controller P89C51RD2 derives its input from ADC and the process value acquired through ADC is compared with a set point to determine the error. It uses the algorithm stored in it to gather the control signal, which is in turn processed to generate the new trigger pulses for the devices in the converter in order to regulate the output voltage and simultaneously improve the input power factor.

The trigger pulses migrate through the opto-coupler and accomplish high-speed logic interfacing, input/output buffering as line receivers in environments that conventional line receivers cannot tolerate. The signals from the opto-coupler are inverted using NOT gate and then fed to the driver to strengthen the PWM pulses.

The Figs. 10 and 11 show the flow diagram responsible for generating the PWM pulses and the experimental prototype. The output voltage and current waveforms seen in Figs. 12 and 13 repudiate the capability of the algorithm to maintain a constant output voltage even when it experiences a sudden disturbance in load. The entries in Table 1 compare the simulated and experimental readings to substantiate the viability of the scheme over a range of operating loads.

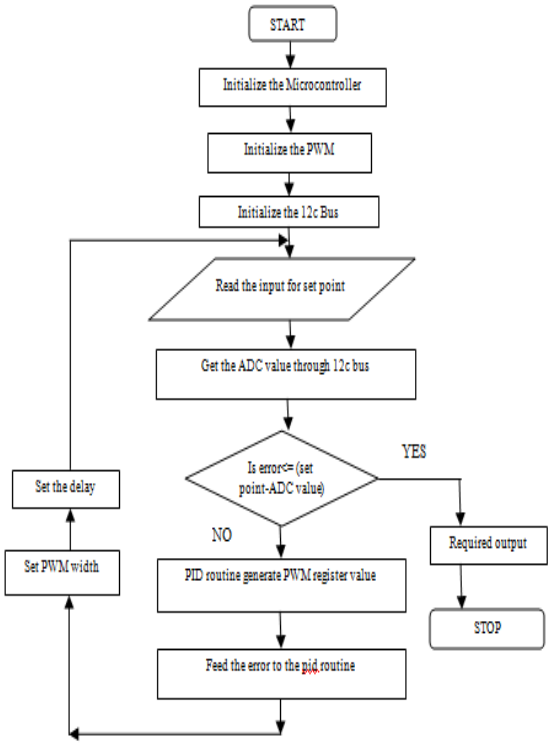

Fig. 10 Flow diagram

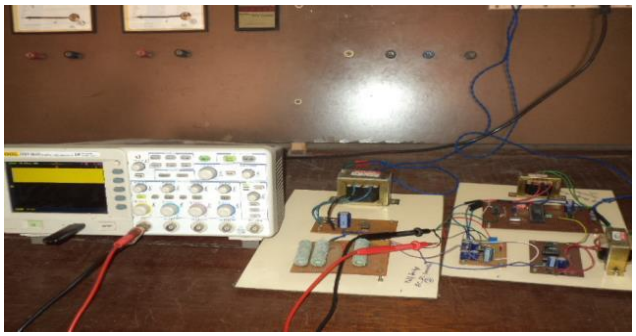

Fig.11 Experimental setup

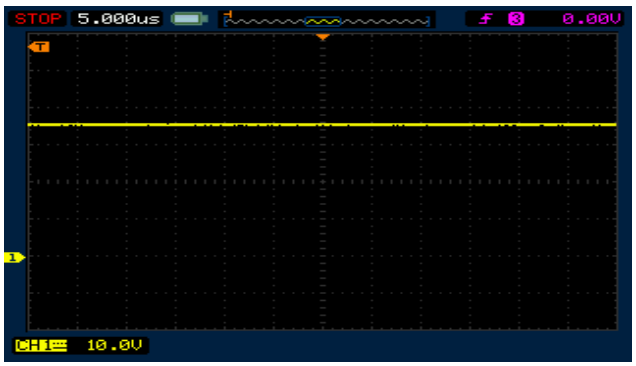

Fig.12 Output voltage waveform

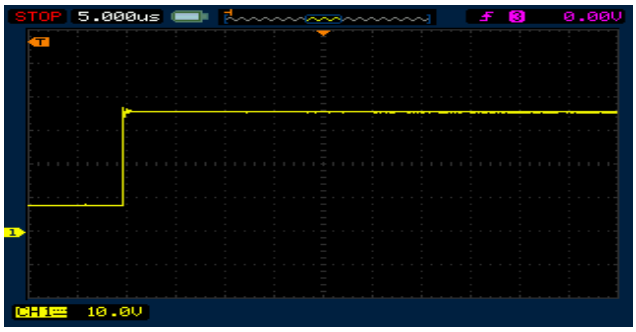

Fig.13 Output current waveform

Table 1. Performance Comparison

Power (watts)	Load Voltage (V)		Load Current (A)	Power Factor	
	SIM	HW		SIM	HW
1000	233.11	229.0	4.45	0.99	0.92
1500	233.02	230.0	6.71	0.99	0.93
2000	232.23	230.0	8.86	0.99	0.94
2500	231.85	229.0	11.25	0.99	0.96
3000	231.36	230.0	13.25	0.99	0.96
3500	230.65	230.0	16.32	0.99	0.97

VII. CONCLUSION

A PWM strategy has been developed to improve the input power factor of a buck boost ac-dc converter. The control algorithm has been evolved as a mechanism to reshape the nature of the actual input current vector. The philosophy has been released using a microcontroller to validate the MATLAB based simulation results. The merits of the methodology will serve to expand the scope of the use of the buck boost converter in the utility world.

ACKNOWLEDGMENT

The authors gratefully acknowledge the authorities of Annamalai University for the facilities offered to carry out this work.

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