A Novel Low Power Fault Tolerant Full Adder for Deep Submicron Technology

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Abstract— A low power and high speed Full adder circuit design using a new CMOS domino logic family is presented in this paper. Compared to static CMOS logic circuits, dynamic logic circuits are important as it provides better speed and has less transistor requirement. The proposed circuit has very low dynamic power consumption and less delay compared to the recently proposed circuit techniques for the dynamic logic styles. Moreover, it will be shown that the proposed circuit is extremely fault tolerant. The monte carlo simulation is performed to emphasis the fault tolerance of proposed full adder. The proposed full adder is simulated using standard 0.18 um CMOS technology.

I.   INTRODUCTION

The static CMOS logic is the best known for its lowest power dissipation but its speed is not so high. On the other hand, as the number of inputs increase, the number of transistors required will be doubled. In order to reduce the transistor count, pseudo NMOS is preferred, whereby area is also reduced. But it fails to improve speed and reduce power dissipation. Since, there is a conflict between the devices in the pull down network and the grounded PMOS load device the nominal low output voltage for Pseudo NMOS is not 0V. As a result noise margins are reduced and static power dissipation is increased [1].

Dynamic logic requires less number of transistors to implement a given logic and is well suited for high speed circuit design. However, the major drawback of this logic is that it has excessive power dissipation due to the switching activity and clock. Some techniques are proposed for reducing excessive power dissipation of dynamic logic circuit. a mix of dynamic and static circuit styles [2], use of dual supply voltages [3] and dual threshold voltage [4] are some of these techniques. In [5] new logic family called feedthrough logic (FTL) is proposed to have better speed and low power dissipation.

On the other hand, in submicron applications the process changes is extremely troublesome. As the oxide thickness in today technology is very thin, its variation is extensive. Changing the thickness of oxide layer can affect the performance of integrated circuits. However, by designing a suitable circuit, the performance of circuit could be independent from process variations.

In this paper, we presented an optimized design for a full adder cell craved for low power, low energy, and fault tolerant. The rest of the paper is organized as follows. In section II, the proposed dynamic logic and proposed full adder is presented. In section III, simulation results are presented. Section IV concludes the paper.

II.   PROPOSED PREAMPLIFIER TOPOLOGY

In this section, a novel technique is proposed to reduce power consumption of domino logic. In proposed circuit, a buffer is used in domino logic circuit causing to reduce the power consumption of proposed logic compared to conventional domino logic circuits. The proposed domino logic circuit is plotted in Fig. 1. The circuits composed of three clock transistor so the load capacitor will be increased. In charge duration that clock is low, M6 is off and the output node would not be changed. When clock is high, M1 is off and M2 is on. In this condition, if the input A is high, M3 is on and the node Z is grounded. On the other hand, if input A is low, the node Z would be high impedance and would not be changed. Similarly, if Z and clock is high the output F is grounded and if Z is high and clock is low the output will be high.
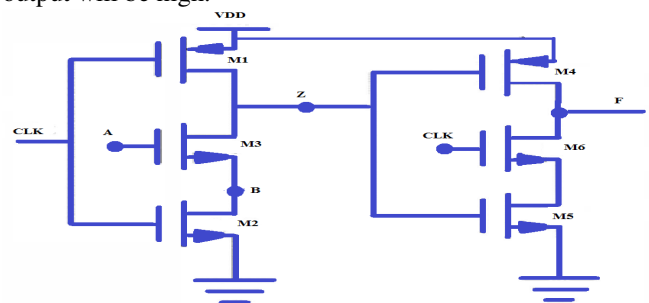

Fig. 1 The proposed domino logic circuit

For the sake of lower power consumption, the proposed domino logic circuit is modified as shown in Fig. 2. In this circuit, the source of M5 is connected to node B instead of ground. So, during charge period when clock is low, the node Z could not be propagated to output. In this circuit, when the input A is low the node Z is always high and the output is always low. When the input A is high, the circuit can work in two different phases.
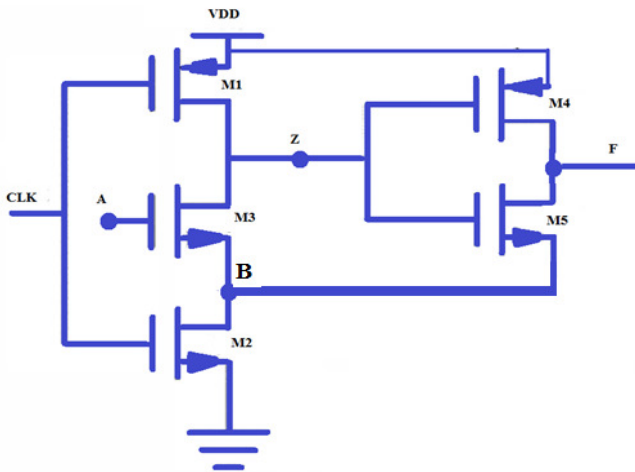

Fig. 2 the modified proposed domino logic circuit

Now that the novel domino logic circuit is designed, it is time to design a novel full adder using this proposed logic. The schematic of proposed full adder is shown in Fig. 3.
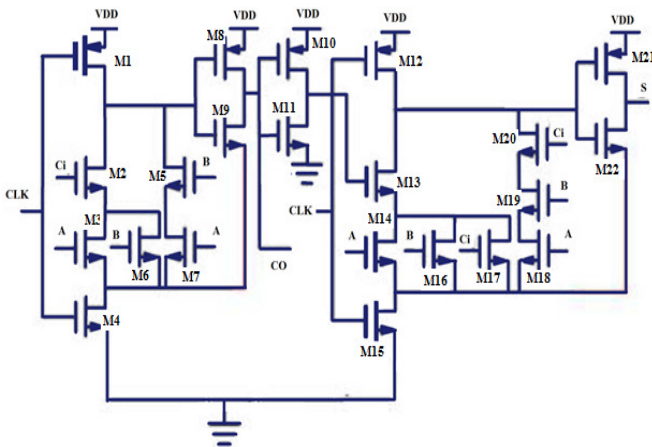

Fig. 3 schematic of proposed full adder

III.   SIMULATION RESULTS

In this section, the simulation results of proposed domino logic and full adder is presented. Fig. 4 shows transient response of proposed buffer.
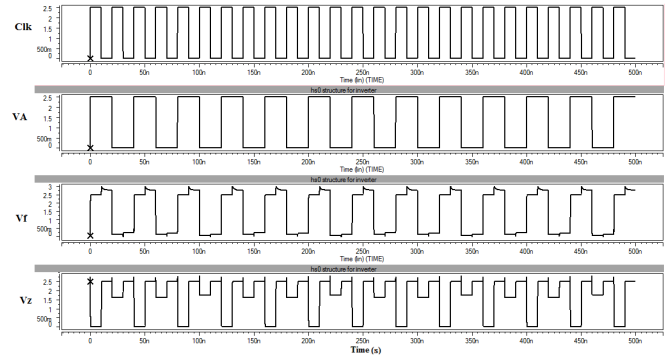

Fig. 4 transient response of proposed buffer

The delay of this buffer is plotted in Fig. 5. On can see that the delay of this circuit is 0.3 ns. Total voltage source power dissipation of this buffer is 42.2089 pW.
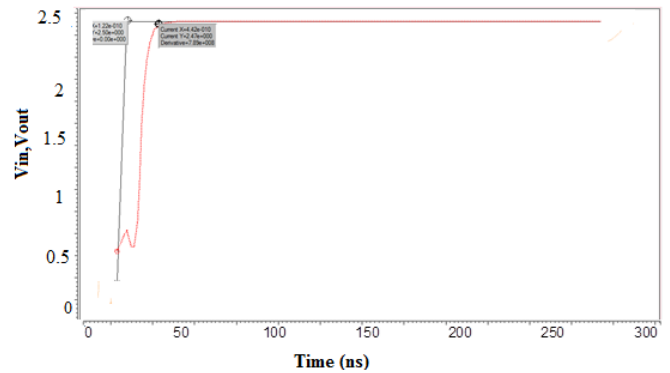

Fig. 5 The delay of proposed buffer

Fig. 6 shows the simulation results of the proposed full adder. One can see that, when all inputs are high, both outputs sum and Cout are high. When two inputs are high and other input is low, one output is low and the other is high.
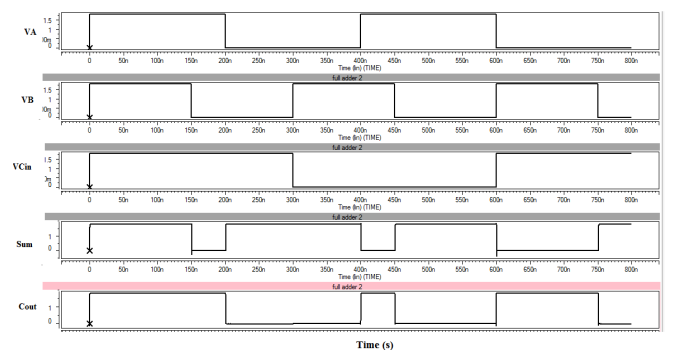

Fig. 6 simulation results of the proposed full adder.

Total voltage source power dissipation of this full adder is 447.8459 pW. The delay of this full adder is plotted in Fig. 7. As is shown in the diagram, the delay of proposed full adder is 0.35 ns.
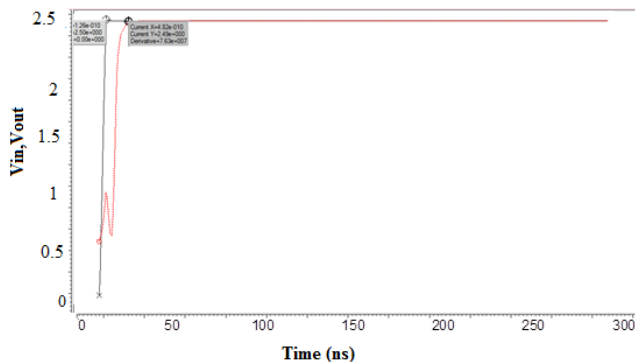
Fig. 7 delay of proposed full adder

To show that the proposed full adder is fault tolerant, different faults including process fault, voltage variations, parasitic capacitors, and noise are injected in the circuit. Fig. 8 shows the simulation result of proposed full adder under the condition that all of fault sources are injected in the circuit simultaneously. One can see that besides injecting all of these faults, the performance of full adder is not changed. The results of injecting fault in proposed full adder is summarized in Table. 1.
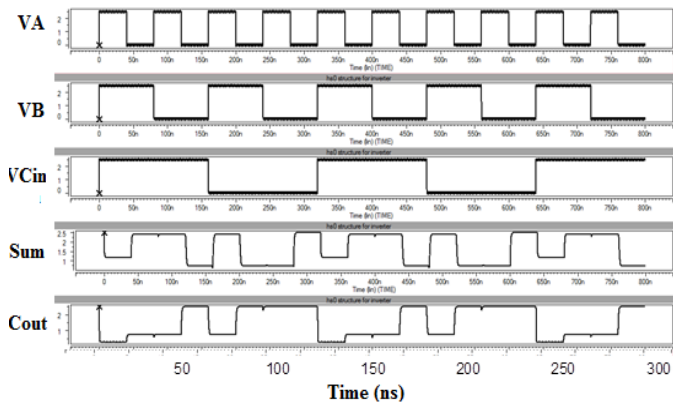

Fig. 8   simulation result of faults injected proposed full adder

Table. 1 results of injecting fault in proposed full adder

Power consumption	Delay	Fault
447 pW	0.35 ns	No fault
447 pW	0.37 ns	Process falt
44 pW	0.4 ns	Voltage variation
447 pW	0.63 ns	Parasitic capacitance
447 pW	0.33 ns	Noise injection

Table. 2 the comparison of proposed full adder with other works is presented.

Table. 2 comparison of proposed full adder

Delay	Power consumption	
0.35 ns	0.447 uW	This work
1.009 ns	1.73 mW	[6]
0.24 ns	4.1 uW	[7]
0.32 ns	4.6 uW	[8]
0.43 ns	5.4 uW	[9]

IV. CONCLUSIONS

This work has presented a novel low power and high speed Full adder circuit design using a new CMOS domino logic family. The proposed circuit had very low power consumption and less delay compared to the recently proposed circuit techniques for the dynamic logic styles. Moreover, it was shown that the proposed circuit is extremely fault tolerant. Different faults including process fault, voltage variations, parasitic capacitors, and noise were injected in the circuit. Besides injecting all of these faults, the performance of full adder was not changed. The proposed full adder consumed only 0.447 uW of power and had the delay of 0.32 ns.

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