IJCSE International Journal of Computer Sciences and Engineering Open Access
Survey Paper Vol.-7, Issue-4, April 2019 E-ISSN: 2347-2693

A Low Power SEU Resilient 13T SRAM using MTCMOS

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DOI: https://doi.org/10.26438/ijcse/v7i4.11201125 | Available online at: www.ijcseonline.org

Accepted: 18/Apr/2019, Published: 30/Apr/2019

***Abstract*— There has been an increasing interest in the radiation immunity of circuits in recent years as modern integrated circuits operating in high radiation environment require careful attention to the soft errors resulting in bit upsets. These events are referred to as single-event upsets (SEUs). SEUs will become more severe as a result of technology scaling and play a pivotal role in memory system stability. Memory systems with lower sensitivity to SEUs offer better stability and reliability if ignored lead to catastrophic situations in fields such as medicine, aerospace, etc. Therefore, it has become crucial that the design of the memory arrays is SEU resilient. The proposed design achieves high soft-error tolerance for robust low power operation in high-radiation environments making use of the MTCMOS technique. Less leakage power consumption is an important reason why this technology is incorporated into larger systems such as memories. This, in turn, leads to improved efficacy along with reduced susceptibility to single-event upsets and lower power consumption.

Keywords*— *Single Event Upset (SEU), rad-hardening (radiation hardening), Static Random Access Memory (SRAM), low power, Multi-threshold CMOS (MTCMOS).

I. INTRODUCTION

As lithography continues to shrink and the operating voltage decreasing drastically, microelectronic devices and circuits tend to steer towards susceptibility to soft errors, especially the ones in a high radiation environment. The ephemeral radiation-induced soft error has now become a key threat. Left unchallenged, they have the potential of inducing the highest failure rate out of all the other reliability mechanisms combined. A proliferation of radiation effects in semiconductor devices that vary in magnitude cause permanent damage ranging from parametric shifts to complete device failure. The primary concern of commercial terrestrial applications is the “soft” single-event effects (SEEs) that are predominant in space and military environments, as opposed to the “hard” SEEs [1].

The natural space radiation environment consists of the protons, electrons, heavier ions and transient particles. Transient radiation consists of Galactic cosmic ray (GCR) particles and particles from solar events, such as coronal mass ejections and flares. Both natural and man-made radiation are present on Earth out of which the sources that are most important in producing effects in microelectronics on the ground outside of nuclear facilities are terrestrial and cosmic rays, which induce single event effects, presenting special radiation effect challenges [2]. Though SEEs became known when Wallmark and Marcus had first predicted in 1970 that cosmic rays would eventually start upsetting microcircuits as feature size shrinks, due to heavily ionizing tracks and cosmic ray spallation reactions, the prehistory of single event upsets (SEUs) dates back to the nineteen fifties.

A. The Genesis of the SEU

During the prehistoric period of soft errors, 1945 through 1957, the first random and unexplained anomalies were observed during above-ground nuclear testing. And in the 1990s, neutrons at aircraft altitudes were recognized to induce SEEs, posing a reliability issue. And the Static Random Access Memory (SRAM) cell became unequivocally the most investigated component in terms of rad-hardening (radiation hardening) as the SRAMs started showing some susceptibility to SEE early on. Since the SRAM blocks occupied the majority of the chip area and were the primary contributors to leakage power, they eventually became the Achilles’ heel for radiation applications requiring SEE immunity [3].

The future progress of integrated circuit technologies impacts SEE tolerance on a variety of levels—potential new material particle emissions, reduced noise margins due to scaling, increased sensitivity due to new circuit topologies, increased operational speed, and the increased probability for errors due to the ever-increasing density of information storage and processing. It is because of this uncertainty that SEU vulnerability has been and continues to be significant in the long haul [4].

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Therefore, addressing the challenges posed by the aforementioned Singe event upsets as discussed in Section 1 and contributions to improve the system performance becomes the base of the paper. Section 2 deals with the different types of radiation effects and the manifestation of the glitch in the circuit. Section 3 provides an in-depth analysis of the MTCMOS technique employed to acutely reduce the overall power consumption, making the design even more robust and resilient. Section 4 presents the outcomes of the various simulations. Section 5 gives the conclusions.

II. Radiation Effects in Microelecrtonics

Radiation effects in electronics are generally classified into two types: total dose effects, typically known as the Total ionizing dose (TID), and single event effects (SEE). TID describes the cumulative effects of charged particles on the doping levels of substrate materials within electronics, specifically silicon. SEE refer to altered circuit functioning as a result of a single charged particle interacting with the internal material of an electronic component [5].
Total ionizing dose (TID) in electronics is a cumulative, long-term degradation mechanism due to mainly protons and electrons depositing charge in electronic components, while a smaller contribution occurs from secondary particles arising from interactions between the primary particles and spacecraft electronics [6] while Single event effects (SEE) are the electrical disturbances caused by energetic charged particles. The passage of a single charged particle through a device or a sensitive region of a microcircuit induces the SEE. These errors can propagate through the device's logic stream and lead to errors such as a pin outputting an incorrect value or a circuit element latching incorrect data. SEEs can manifest in several forms, they are divided into three main categories according to the consequence of the spurious current pulse. SEEs in Electronic Devices group are the possible effects induced by the interaction of a nuclear particle with the electronic components.

(i) SEUs in SRAM

For the last few decades as a result of the development of microelectronics, the dimensions of MOS devices are shrinking. Therefore, reliability becomes a serious concern, especially at the nanoscale dimension. The conventional 6T as shown in Figure 1 is highly sensitive to SEUs, as any upset that causes one of the data nodes to cross the switching threshold of the adjacent inverter will result in a bit flip. [7]
When operating at low voltages, the switching threshold decreases, thereby increasing the soft-error susceptibility because of the active feedback loop between two cross-coupled inverters. The typical cross-coupled inverter structure cannot achieve sufficient radiation tolerance under low supply voltages. As SRAM blocks occupy the majority of the chip area, the probability of a radiation strike on an SRAM bitcell is relatively high due to the large area of the SRAM core. Therefore, SRAM soft-error mitigation has become essential for robust system design.
To demonstrate an SEU causing a failure in 6T SRAM bitcell, the following example will assume that an energetic particle strikes a circuit storing a logic 1 (Q = VDD and QB = 0 V). If the particle strikes the drain of the cutoff PMOS transistor, M3, and a charge will be generated, temporarily changing the state of QB. For notation purposes, we will refer to this type of positively charged strike as a 0 to 1 upset at node QB, as opposed to a negatively charged strike, which we will refer to as a 1 to 0 upset at this node. Before the deposited charge can be evacuated to the power supply through the conducting transistor of the feedback inverter (M1), the feed-forward inverter (M2 andM4) switches and discharges Q. This, in turn, enforces the wrong state at QB, thereby latching the error into the memory cell.

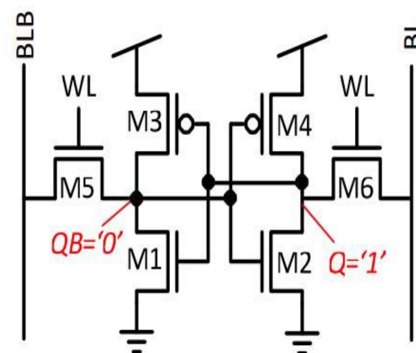

Figure 1. Conventional 6T SRAM cell.

The 13T bitcell, shown in Figure 2, achieves radiation hardening by employing a dual-feedback, separated storage mechanism to overcome the increased vulnerability due to supply voltage scaling. The storage mechanism of this circuit comprises five separate nodes: Q, QB1, QB2, A, and B, with the acute data value stored at Q. This node is driven by a pair of CMOS inverters made up of transistors N3, P3, N4, and P4 that are respectively driven by the inverted data level, stored at QB1 and QB2. QB1 and QB2 are respectively driven to VDD or GND through devices P1, P2, N1, and N2 that are controlled by the weak feedback nodes, A and B, that are connected to Q through a pair of complementary devices (P5 and N5) gated by QB2. By driving the acute data level with a pair of independent inverters, a strong, dual-driven feedback mechanism is applied with node separation for SEU protection. This setup effectively protects Q from an upset on QB1 or QB2, while achieving a high critical charge at node Q.
A couple of write access transistors (N6 and N7) tend to connect write bitline (WBL) to nodes A and B. These devices are controlled by a write wordline (WWL), such that when WWL is raised, both A and B are pulled toward the

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level driven upon WBL. This virtual connection between A and B creates inverters out of the transistor pairs of N1, P1 and N2, P2, driving QB1 and QB2 to the opposite level of WBL. Accordingly, the written data level is driven back to Q through the dual-driven feedback inverters, bringing the cell to a stable state. Nodes A and B are driven to a predetermined level during the write operation and therefore are not reliant on the aforementioned leakage currents to set the initial storage level of the cell. [8]

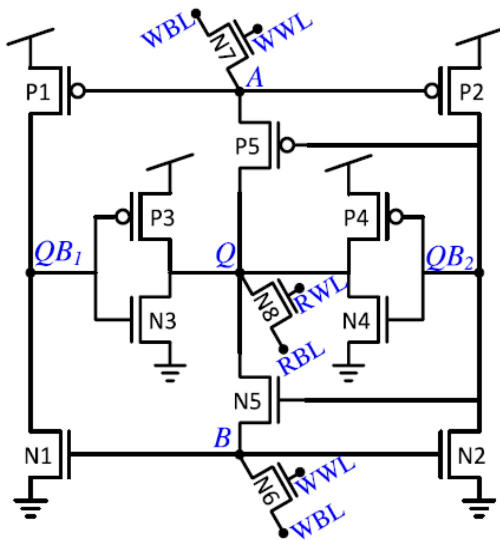

Figure 2. Schematic of the 13T SRAM bitcell.

The 13T SRAM bitcell features single-ended readout through the read access transistor (N8). This device is controlled by a separate read wordline and connected to a column-shared read bitline that is pre-charged prior to the read operation and conditionally discharged, depending on the voltage stored at Q. Due to the dual-driven feedback that drives Q to its stable value, this read operation is both more robust and faster than the read operation of the standard SRAM bitcells, however a half-select situation will indeed occur during a partial row write.

III. 13T SRAM USING MTCMOS TECHNIQUE

With the increasing prominence of prolonging battery life as much as possible for space applications, strict demands on the overall power consumption are imposed. Although the battery industry has been making efforts to develop batteries with a higher energy capacity, a revolutionary increase in the energy capacity does not seem imminent. Another important reason for low-power design is reliability. Scaling of technology not only increases power density, but also the current density. Large current densities cause serious problems increasing the heat gradient across the chip, causing thermal and mechanical stress leading to early breakdown. [9]

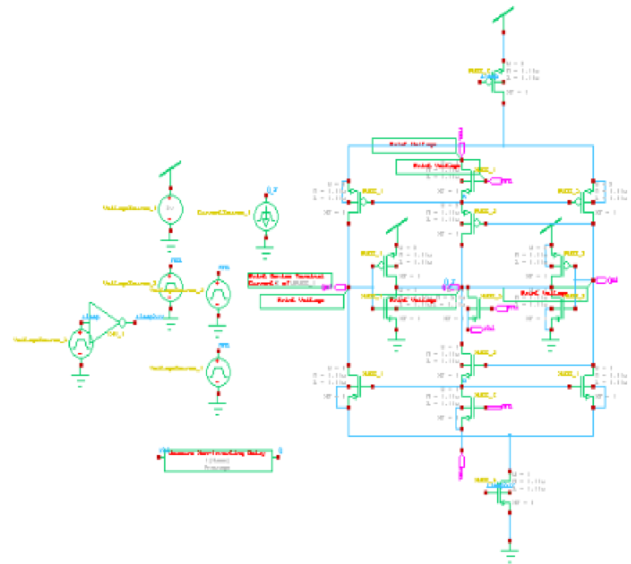

Figure 3. Schematic of the 13T SRAM.

Figure 3 shows the schematic of the radiation tolerant 13T SRAM. A supply voltage of 2V and dynamic inputs RBL, WBL and WWL are given to the circuit. Read and write operations are performed on the 13T SRAM.

(i) Power Gating

When space applications are in an idle state, when no computations are being performed, it is very wasteful to have such large sub-threshold leakage currents. This static power dissipation occurring in the standby mode could be reduced dramatically by the usage of high V_{th} transistors. In addition to this, circuits can easily be placed in low leakage states at a fine grain level of control. For this reason, and because it is less susceptible to, soft errors, MTCMOS technique is suitable for space applications in a high radiation environment.

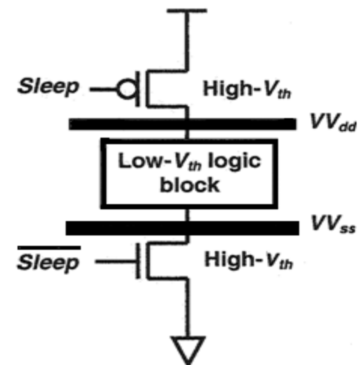

Figure 4. Generic structure of MTCMOS.

In the active mode, when Sleep is set low, the high V_{th} transistors are turned on and the on-resistance is so small that VV_{dd} and VV_{ss} are connected to main supply and ground

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lines through the high V_{th} transistors and function as real power lines. Therefore, the low V_{th} logic block operates normally and at a high speed because the V_{th} is low enough, relative to the supply voltage. And in the sleep mode, when Sleep is set high, the high V_{th} transistors are turned off causing the virtual lines VV_{dd} and VV_{ss} to float which limit the leakage current to that of the high V_{th} transistors. The relatively large leakage current determined by the sub-threshold characteristics of low V_{th} MOSFETs is suppressed by the sleep control transistors as they have a high V_{th} and thus a much lower leakage current. Therefore, power consumption during the standby period is significantly reduced by the sleep control. [10]

The schematic of 16x16 13T SRAM using MTCMOS is designed using Tanner EDA as shown in Figure 5. A supply voltage of 2V and 16 inputs of RBL, RWL, WBL and WWL and additional sleep control signals, sleep and sleep bar are given to the circuit to operate in active and sleep modes.

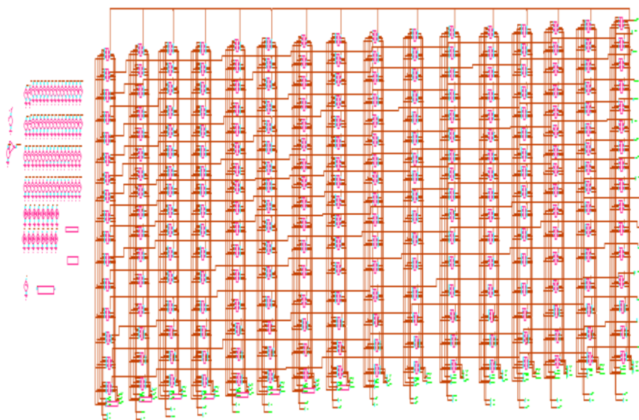

Figure 5. Schematic of the 16x16 array.

(ii) Disrupt Modelling

The 13T bitcell is robust with upset tolerant operation in a high-radiation environment, such as that encountered by space applications. When a particle strikes, the characteristic of such an environment, passes through a semiconductor material, disrupts occurs due to the drift current of the generated e–h pairs in a reverse biased p-n junction. [11] If the particle hits an unbiased junction, the generated e–h pairs will spontaneously recombine and not induce a current pulse due to the absence of an electric field. However, a strike on a reverse-biased junction causes a transient current [I (t)] at the connected node, characterized by a fast rise time and a gradual fall time disrupting the tolerance of the bitcell. [12]

The charge collected due to the particle strike depends on the type of the ionizing particle, trajectory, energy value, and impact location. The critical charge is calculated from the numerical integration of the injected current pulse that causes a bit flip. Two basic principles provide the bitcell with inherent SEU tolerance. (a) The data are read out from node Q, such that any temporary upset on other nodes can be tolerated. (b) The assisting nodes are designed with redundancy to ensure that any upset will be mitigated by the other nodes. When a radiation strike causes a value change on any node of the bitcell, the other four internal nodes are designed, so that the state change at this node cannot flip the cell and the disruption is suppressed within a deterministic time. For example, an upset at Q will quickly be suppressed through the dual-driven mechanism created by the internal inverters. [13] Due to their separated nature, upsets at QB1 and QB2 will not be able to change the state at Q and will return to their original state. Two important parameters to evaluate the tolerance of a bitcell for particle strikes when operating in a high-radiation environment are recovery time and critical charge. The recovery time is the time it takes Q to return to its correct readable data value following a particle strike, while the critical charge is the minimum charge required to cause a bit-flip. A correct readout only requires the data to be stable at node Q, and therefore, it is sufficient to consider the voltage at this node for such an evaluation. Figure 3.3 shows the reaction of the internal nodes combating single event upsets when particle strike occurs at the storage node Q. And recovery of the acute data stored at Q from single event upsets. [14]

IV. SIMULATION RESULTS

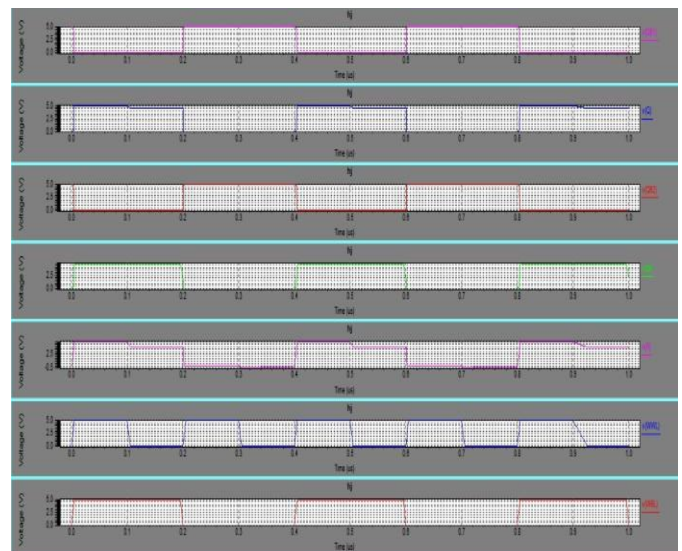

Figure 6. Read-Write operation of the 13T SRAM.

A supply voltage of 2V and dynamic inputs RBL, WBL and WWL are given to the circuit. Read and write operations are performed on the 13T SRAM.

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Figure 7 shows the standby mode of operation of the 13T SRAM with MTCMOS. Sleep is at 1 and the circuit holds the output of the previous state

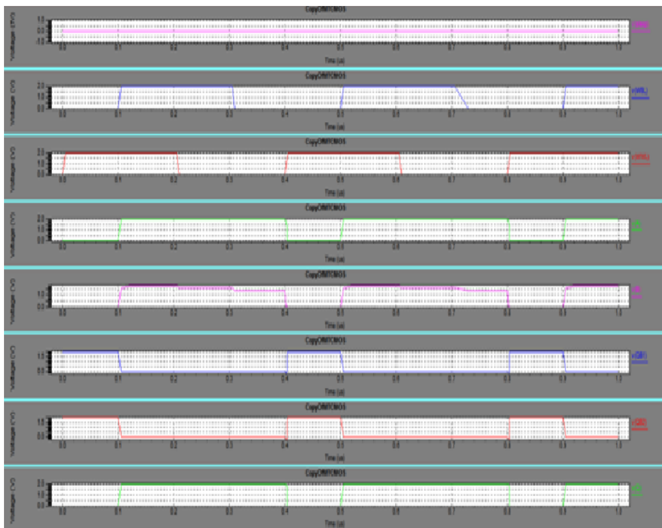

Figure 7. Active mode of operation of the 13T SRAM with MTCMOS.

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The SEU tolerance of the 13T SRAM with MTCMOS is checked by injecting a current pulse at one of the nodes. But, as a correct readout only requires the data to be stable at node Q, therefore, it is sufficient to consider the voltage at this node for such an evaluation.

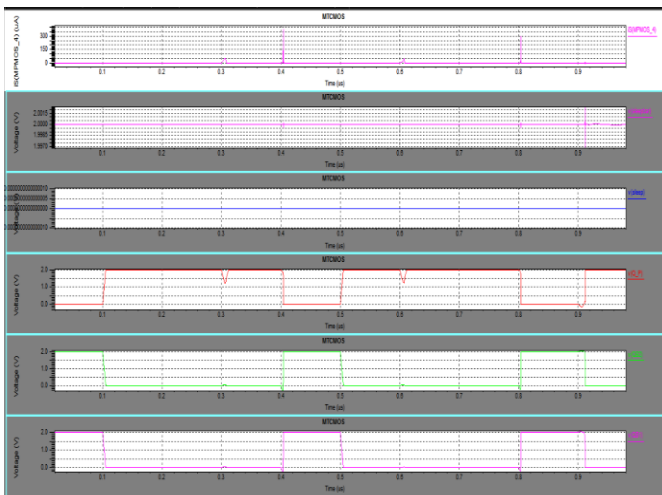

Figure 8. SEU tolerance of 13T SRAM with MTCMOS.

Figure 8 shows the reaction of the internal nodes combating single event upsets when the particle strike occurs at the storage node and recovery of the acute data stored at Q from single event upsets.

Figure 9 shows the recovery of the 16X16 13T SRAM with MTCMOS from SEU's in active mode. Voltage rise and drops are quickly restored, retaining the actual data value, avoiding an erroneous data read during the read access.

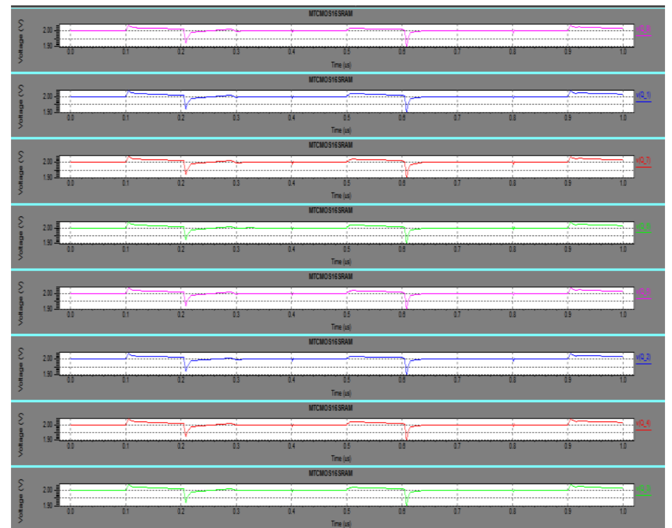

Figure 9. SEU resilience of the 16x16 array.

Figure 10 shows the graph plotted between average power consumption and temperature of the 13T and the 13T SRAM with MTCMOS during read-write operations.

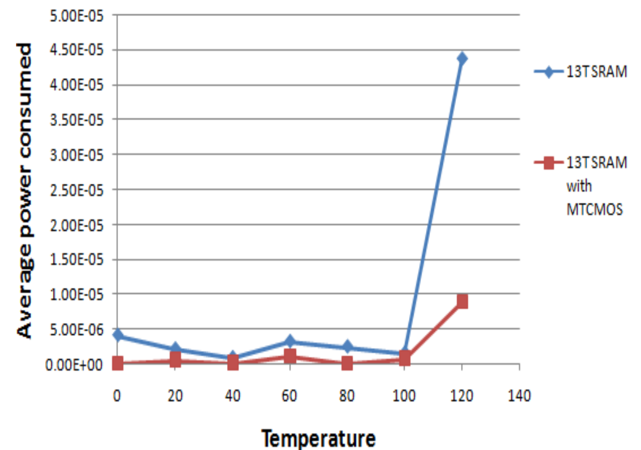

Figure 10. Power consumption vs temperature of the 13T and 13T SRAM using MTCMOS.

V. CONCLUSION

The 13T SRAM using MTCMOS displays a novel dual-driven separated feedback mechanism to achieve high soft-error tolerance, for robust low power operation in high-radiation environments. Particle strike suppression was tested showing tolerance to upsets with reduced recovery time, enhancing the robustness of the cell. The power delay product of the circuit is reduced improving the stability when compared to the previous 13T radiation tolerant bitcell. The

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power consumption of the circuit is significantly reduced while performing read and write operations as well as in sleep mode, prolonging the battery life of the application along with a decrease in delay, improving the performance of the 13T SRAM bitcell by using the MTCMOS technique.

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