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To Design Low power Magnitude Comparator using CMOS Technolgy

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***Abstract*—** This paper presents a low power 2 bit magnitude comparator. The speed and power of comparator have important influence on performance of complex arithmetic and logical circuitries such as ADC, Memory chips etc. It plays a vital role in various DSP, high speed data processors, microprocessors, microcontroller based applications. The proposed comparator design is compared with different logic styles such as PTL, Domino logic, and Transmission gates with voltage sweep. The simulations are carried out on Mentor Graphics (ELDO tool) using 90 nm technology and in Micowind using 180 nm technologies. Simulation is done on 0.6V, 0.8V, 1V and 1.2V respectively. It is found that power is least dissipates in 0.6 V that is 48.82pW.but it has the longest delay of 53.098ns.The simulation results of proposed design using 90 nm technology show improvement in power delay product, 60.26% in greater than circuit, 56.14% in lesser than circuit and 59.48% in equals to function.

***Keywords*—**Magniude Comparator, CMOS technology, Domino logic, PDP,Coupling

I. INTRODUCTION

Now a day's low power design and high throughput is need of an hour. As there is need of fast electronic devices such as Low-Power Data Acquisition, Battery-Powered Handheld Equipment, Level Sensors, Ultrasonic Flow Meters, Motor Control, Wearable Fitness. The magnitude comparator use various logic gates such as AND, OR, EX-OR, NOT etc. for a design. To compare various digital input signals.

The magnitude comparator (Figure1) is the electronic device that takes input in the form of binary number and determines the comparison result whether the signals are greater than, lesser than or equals to as compared with each other.

Now the speed of system can be easily increased by reducing gate length. Circuit size relies on the quantity of transistors and their sizes and on the wiring complexity. To design a system with low power consumption designer use Complementary Metal Oxide Semiconductor (CMOS).CMOS contains combination of both PMOS and NMOS. [1]

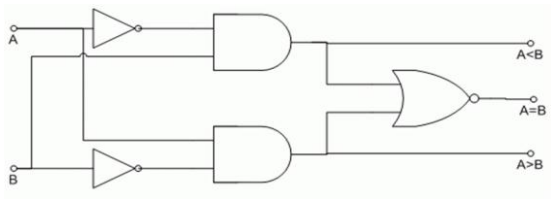

Figure 1: Comparator basic Circuit

Section II contain the related work of comparator Design, Section III contain methodology used for the comparator design that is design using domino logic, simulation circuits for each function. Section IV contains the results for the circuits using VDD 1.2V. Section V concludes research work with future directions

II. RELATED WORK

In paper [1] A Design of low power magnitude comparator, design of magnitude comparator using domino logic is presented. Performance parameters are increased in terms of power, power delay product as compared to simple circuit. 90nm technology is used to get power dissipation parameter reduced to Pico Watts. Design is simulated for different voltage sweeps from 0.6V to 1V.

In paper [2], 'the design of low power high speed comparator using 0.13um CMOS', the design of comparator is designed using 0.13um technology. Power dissipation is only 1.5nW. It works on supply voltage of 1.2V.

In paper [3], 'Design of A Low Power 0.25 µm CMOS Comparator for Sigma-Delta Analog-to-Digital Converter', application of comparator for ADC design is discussed. Dynamic latch method is used to design comparator. This design is used for high speed ADC. Overall result of the power dissipation is slightly off than the targeted value

In paper [4], 'Comparative Analysis of a 2-bit Magnitude Comparator using various High Performance Techniques', various logic styles for comparator design like Basic CMOS, Hybrid PTL, Domino etc. are implemented and compared. Hybrid PTL is derived as a Lowest Power consumption technique.

In paper [5], 'Design of low power two bit magnitude comparator using adiabatic logic', zero loss of heat is implemented in 0.18um technology. Power efficiency (PDP) as compared to conventional design is improved and equals to 80.54% as expected theoretically.

III. METHODOLOGY

We can design a comparator using Static CMOS, Ratioed Circuits, Cascode Voltage switch logic, Dynamic Circuits, Pass-Transistor Circuits. Here comparator is designed with the help of Domino logic.

For a two bit comparator if we assume a binary numbers A and B then comparison of these two bits are denoted as, E for equals to result, L for lesser than result, G for greater than result as shown in Table 2

Table 1: Truth table for a 2-bit magnitude Comparator

A1	A0	B1	B0	E	L	G
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

Thus by studying this truth table we can observe that if A bit is greater than B bit then G will be high. If A is lesser than B then L will be high. If A is equals to B then E will be high.

Design of the comparator for the specification of above truth table is done using a Mentor graphics Eldo Tool on 90nm technology. Figure2 Describes the circuit diagram for Equals to Function.

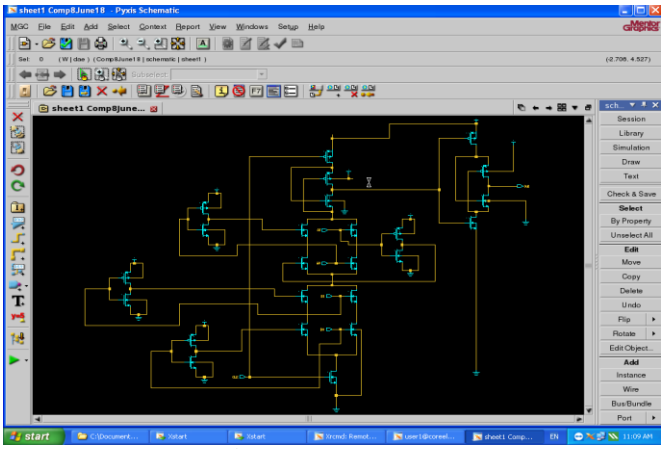

Figure 2: Circuit Diagram for Equals to Function

Figure 3 Describes the circuit diagram for Greater than Function. Figure 4 Describes the circuit diagram for lesser than Function. Simulation Process consist symbol generation and the parameters such as voltage sweep, Gate length, Delay, Pulse width. Figure 5, Figure 6, Figure 7 describes the simulation circuits for the Equals to Circuit, Greater than and Lesser than Circuits.

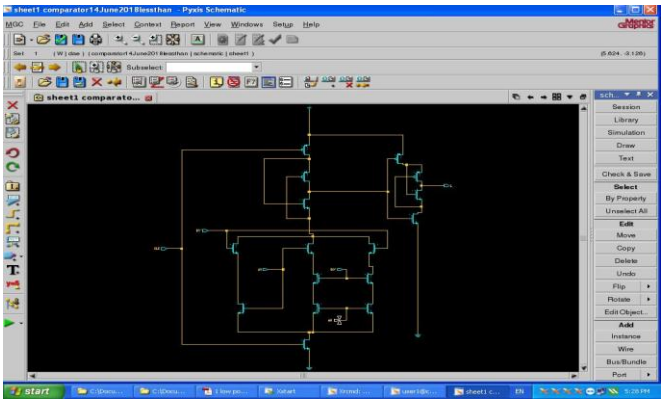

Figure 3: Circuit Diagram for Greater than Function

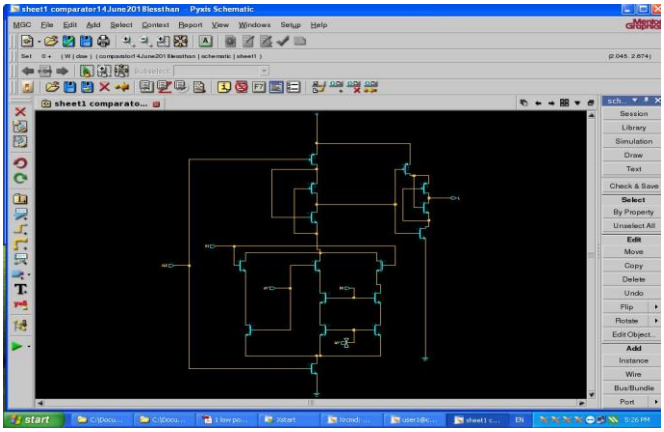

Figure 4: Circuit Diagram for lesser than function

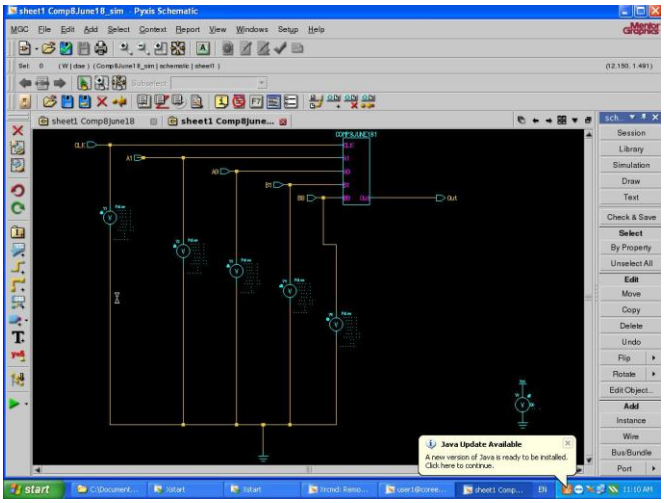

Figure 5: Simulation Circuit for Equals to Circuit

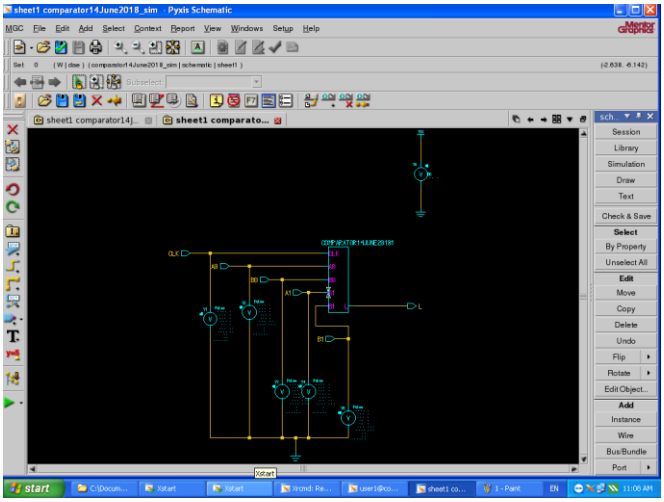

Figure 6: Simulation Circuit for Greater than Function

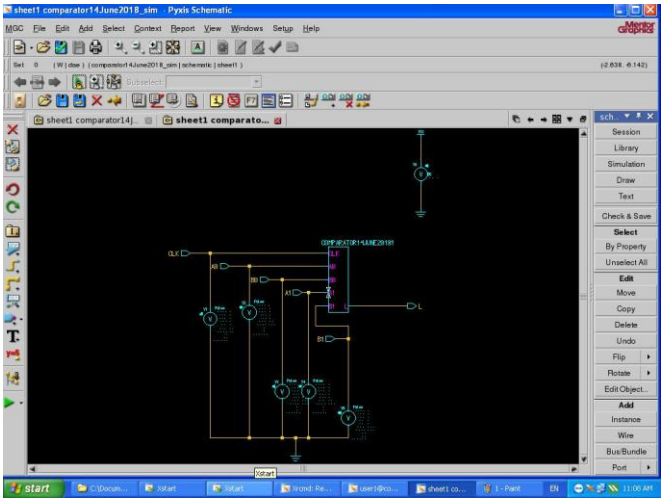

Figure 7: Simulation Circuit for Greater than Function

IV. RESULTS AND DISCUSSION

The transient and DC Analysis are carried out for each circuit using EZ wave Tool. Figure 8 represents the transient analysis for Equals to circuit and Figure 9, Figure 10 represents the Transient analysis for Greater than and Lesser than Circuit.

Table 2: Power Consumption Analysis

Voltage (V)	Power Consumption				
	Basic CMOS (uW)	*Full Adder (uW)*	*Transmission gates[(uW)*	*PTl (uW)*	*Domino Logic (pW) (THIS WORK)*
0.6	*0.5*	*10.6*	*3.8*	*0.8*	*48.8218*
0.8	*1.3*	*33.5*	*10.7*	*3.7*	*73.5868*
1	*4.8*	*85.5*	*23.5*	*10.4*	*110.2903*
1.2	*6.2*	*-*	*44.6*	*11.3*	*197.20*

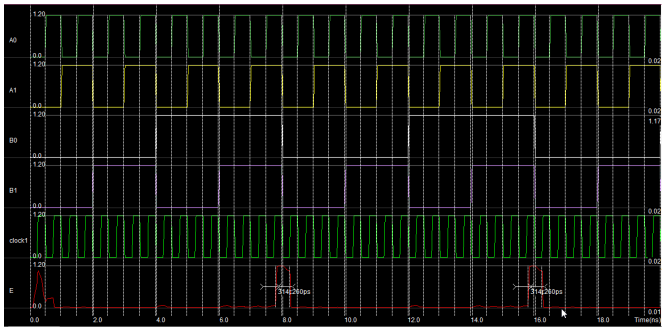

Figure 8: Equals to Circuit Result

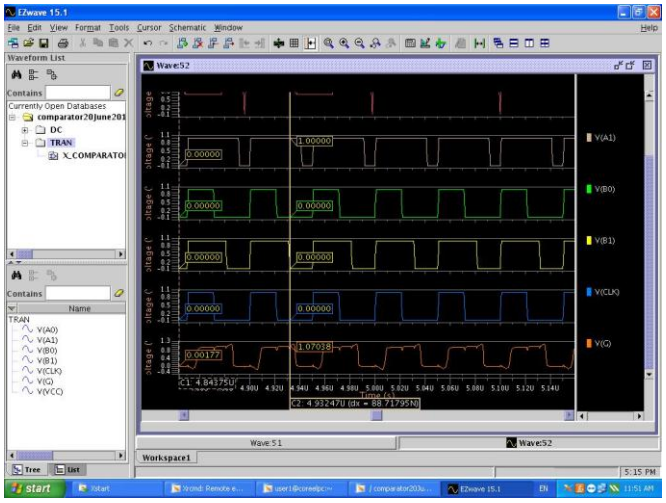

Figure 9: Greater than Circuit Result

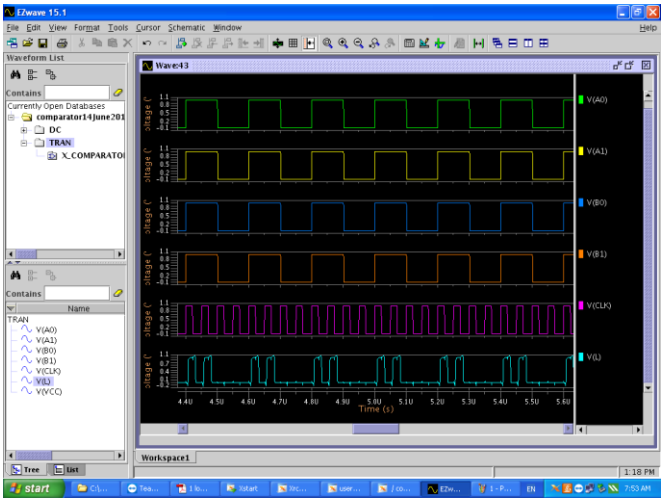

Figure 10: Lesser than Circuit Result

V. CONCLUSION and Future Scope

The comparator is designed for the power and delay optimization. In the present circuit by decreasing the value of VDD the power consumption goes on decreasing but delay increases. The simulation results of the magnitude comparator circuit are in good agreement in terms of power consumption at percentage of 60.26%,56.14% and 59.14% respectively for 'greater than', 'lesser than' and 'equals to function' compare to basic Comparator Design. Also the other parameter shows the improvement in their values..

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