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# Analysis of Power Consumptions in 8 Port NOC Router for Different Topologies

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***Abstract*—**The network on chip (NoC) has replace traditional system on chip (SoC) to meet the communication requirement. The communication on NoC chip is carried out by means of router. For implementing better NoC, the router should be efficiently designed. The paper reviews NoC router and NoC parameters which affects the router design. Design of NoC router depends on network topology, switching techniques and routing algorithm. The Eight port router for different topology design is synthesized and simulated using Verilog code. A comparative study is made on the based of power analyses for different topologies of the 8 port NoC router. It is observed that design of 8 port routers of Octagon, Mesh, Ring, Star, and Torus are having same leakage power. It has been observed that Star topology is less in power consumption as compared to Octagon, Mesh, Ring, Torus and Fat tree topology for 8port NoC router.

***Keywords*—** Network on chip (NOC), Systen on Chip(SOC), Topologies

## I. INTRODUCTION

Network on a chip is the most spectacular electronics device. Networks on Chip (NoC) is playing important role in development in VLSI. Various networking theory methods are used for on-chip communication. Application Specific Routing Algorithm is also a type of algorithm for NoC communication [1]. SoCs can be structured, and reusable and can also improve their performance by NoCs [2]. The solutions to overcome the limitations in NoCs are yet to be presented. Different topologies with different application have been proposed for NoCs including Mesh topology [3], Torus topology, Octagon topology [4], SPIN topology [5], and BFT topology [6]. The main aim of the topology is to improve network performance by providing better static topological characteristics such as diameter and average inter-node distance [7]. When designing the communication NOCs topologies, it is important to consider all the effect of physical problems that face in such as wire routing, wiring density, and power consumption etc [8, 9,10].

## II. NOC TOPOLOGIES

NOC topology defines how the network nodes are connected to each other and determine system cost, as well as Performance for the network. It has a great impact on the system performance and reliability. Selection of appropriate topology can help to improve the performance of chip communication. In a full mesh network, each network node is connected to every other node in the network. Due to this arrangement of nodes, it becomes possible for a simultaneous transmission of data from one node to several other nodes. Some routing algorithm is required for mesh network so that the data traveling over the network take the shortest distance during each of the transmission in different nodes. Mesh shape network consists m columns and n rows and at each intersection, a router is situated and this router is connected to the adjacent router, it is a simple type of topology and easy to implement. In two dimension Torus topology, the network is arranged in a rectangular form of having rows and columns, with each network connected to its four nearest neighbors, and corresponding nodes on opposite edges connected. A network topology where the entire individual network is connected to a central hub or switch is called Star topology. The connection of these individual networks to the central hub or switch is in a form similar to a star structure. Star topology is also known as a star network. It has the ability to limit the impact of a single failure. In star networks, if the central hub or switch got fail then all network will go on fail. Ring topology is a specific kind of network structure in which individual network devices are connected in a ring structure and pass information to or from each other according to their adjacent proximity in the ring structure.

 

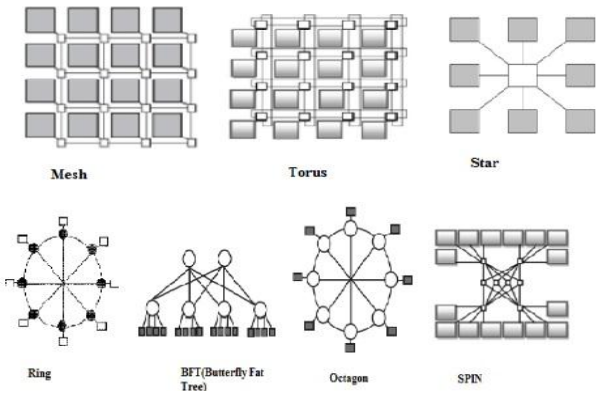


Figure 1: NoC Topologies(source: A Comparative Study of Different Topologies for Network-On-Chip Architecture**,** Sonal S. Bhople, M. A. Gaikwad B.D.C.E. Sewargram, Wardha(M.S.)

Ring topology is highly efficient and handles heavier loads better than bus topology. In-ring topology messages are passed to each individual network in the ring form in clockwise or in anticlockwise. Binary Tree Topology (BFT) has a central root node that is connected to one or more nodes of a lower hierarchy. Scalable Programmable Integrated Network (SPIN) architecture. In this topology router in each level consists of the same number of main ports and sub-ports. This type of topological structure provides higher throughput compared with Butterfly Fat Tree Topology. Octagon Topology is one of the types of the ring topology. It consists of several eight paths so it is called an octagon.

## III. RELATED WORKS

Network delay is a major design parameter for Networks-on-Chip (NoC)-based applications. NoC delay could be achieved at different design phases. The impact of the network topology on NoC system delay using graph-theoretic concepts is given by the Ahmed A. Morgan, M. Watheq El-Kharashi, Fayez Gebali, Haytham Elmiligi [11]. In this paper, the Authors developed a topology based model to calculate the average NoC delay, which is caused by links and routers. The model could be used to select the optimal topology that achieves the minimum network delay for a given NoC application. A study of MPEG4 video application is used to explain how the proposed model could be used to minimize the network delay by selecting the best topology. Results show that a wrong topology leads to the average network delay of the router. Khalid Latif, Tiberiu Seceleanu, Hannu Tenhunen," Power and Area Efficient Design of Network-on-Chip Router Through Utilization of Idle Buffers" [12] explain about the utilization in the idle buffer for the efficient design of NoC router. Cheng Liu·, Liyi Xiao, Fangfa Fu, "Design and Analysis of On-Chip Router" [13] in this paper it analyzes the router consumption resource and designs the router at best cheap cost. W. Zhou, Y. Zhang, and Z. Mao," An application specific NOC mapping for optimized delay [14]. In this paper, an application has been explained for minimizing the delay in NoC mapping. M. Nickray, M.Dehyadgari, and A. Afzali-kusha, "Power and Delay optimization for a network on chip, [15]. In this paper, it introduced an algorithm which is based on genetic algorithm for optimizing power consumption and delay of applications topology. In this paper developed a NOC transmission model of power to calculate the power used during transmission. The logic consists of Vertex mapping to processing elements**,** Node mapping, and latency optimization. These steps map task graphs into a fat-tree NOC how had been minimum power consumption. An algorithm was proposed in this paper could be applied to various derivatives of fat-tree topology. H. Elmiligi, A. A. Morgan, M. W. EI-Kharashi and F.Gebli[16],"A reliability-aware design methodology for network-on-chip applications" explain about different topologies advantages and the parameters. M. Mirza-Aghatabar, S.Koohi, S. Hessabi, M. Pedram. [17], a comparison is done in mesh and torus, in terms of the different application of advantages examples latency, power consumption, and power ratio under different routing algorithms and two common traffic models, uniform and hotspot. And in the comparison torus topology is found to be the best as compared to the mesh with respect to their performance and power consumption. Torus has the high delay as compared to mesh topology. Victor Dumitriu and Gul N. Khan, "Throughput-Oriented NoC Topology Generation and Analysis for High-Performance SoCs", [18]. The Author proposes two algorithms that attempt to meet the communication requirement of an on-chip application using a minimum number of network resources for the task, by generating application-specific topologies. The process of design is difficult to understand. The analysis method which is predicted is used to determine the minimum frequency of different topologies and is incorporated into the topology generation process. And they used this method in real-time applications in MPEG4 decoder and a Multi-Window Display application. The results were found to offer similar or better performance when compared with regular different topologies. Mahmoud Moadeli1, Ali Shahrabi, Wim Vander bauwhede1, Mohamed Ould-Khaoua[19]. It describes the architecture and implemented a model for calculating the average message delay in the spidergon architecture by using the wormhole switching. The simulation experiments result has shown the analytical model predicts the message latency with a good accuracy in a wide range of traffic rates. Ville Rantala, Teijo Lehtonen, Juha Plosila, 'Network on Chip Routing Algorithms[20]. In this paper the Author proposed the router architecture on the basis of routing algorithm.K.Shiney, .K.V.Subrahmanyam and S Chandra Sekhar [21] explain the latest verification methodology of router design.

 

## IV. SIMULATIONS RESULT

### A. SIMULATION IS DONE IN XILINX ISE 14.3 TOOLS

Device specification is as

- Family- Vertex5
- Part –xc5vlx110t
- Package-ff1136
- Speed grade -3

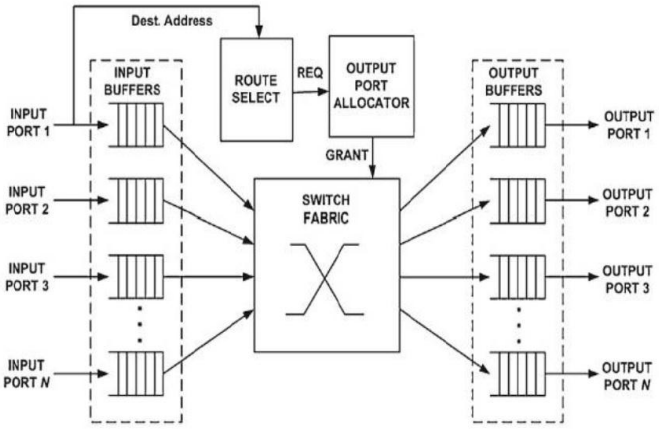


Figure 2: Generic router block diagram

Design of an 8 port Router Architecture consists of 8 port router whose microarchitecture includes of FIFO (First In First Out) Input Buffer, State Modules, Round Robin Arbiter, Encoder and Crossbar Switch each in a port of the 8 port Router. The first stage of the router consists of an input buffer to store the incoming flits that make up the massages. The header bits of each flit is supplied to the state module which determines the type of the flit (head flit, body, or tail flit), and the output destination of massage. Once the output port has been determined using a lookup table, a request signal (req) is sent to the Round Robin Arbiter. After arbitration, the arbiter sends a grant signal to the flit can traverse through the crossbar and reach its destination. At the same time, the arbiter also sends a credit signal to the corresponding input port to release one flit in the buffer so that a new flit can take its place.

### B. OCTAGON 8 PORT RTL SCHEMATIC AND SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Router on Octagon Topology. Here figure shows the 8 port Router for Octagon topology RTL Schematic and simulated waveform. Design of an 8 port Router Architecture will consist of 8 port router whose microarchitecture includes of FIFO (First In First Out) Input Buffer, State Modules, Round Robin Arbiter, Encoder and Crossbar Switch each in a port of the 8 port Router. The first stage of the router consists of an input buffer to store the incoming flits that make up the massages. The header bits of each flit is supplied to the state module which determines the type of the flit (head flit, body, or tail flit), and the output destination of massage. Once the output port has been determined using a lookup table, a request signal (req) is sent to the Round Robin Arbiter. After arbitration, the arbiter sends a grant signal to the flit can traverse through the crossbar and reach its destination. At the same time, the arbiter also sends a credit signal to the corresponding input port to release one flit in the buffer so that a new flit can take its place

Figure 3: Octagon RTL Schematic


Figure 4: shows the simulated waveform of Octagon topology

The Figure shows the simulation result of 8 port NoC router architecture for octagon topology. The rest signals must be kept low during normal operations. The write signals when enabled by the corresponding input signals or the data packets to be given to the router. The routing pattern is observed from the output signals. The output singles follow the round robin scheduling algorithm. The data at the input ports are directed to the output port depending on the first three bits of the input data which act as the select lines. Since the design of 8port Router is octagon topology thus we can say that input port of port1 goes to port2, port8, and port5. Routes to every output of the routers are through the

 

select lines. For an instance lets we want to route a packet from port1 to port2, port8, port5 then for the given design specification when a clock pulse is applied at a time period of 10 ns for the input applied at input port 1 is 01000011. In this design specification to get the input at port 1 to be routed in port2, port8, port5. First select line sel1 is fed the value as 000110. It can be observed that the output at port2, port8, port5 is obtained. Thus we can say that the data packets have been successfully routes.

### C. MESH 8 PORT SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Router on Mesh Topology. Here figure show the 8 port Router for Mesh topology simulated waveform


Figure 5: shows the simulated waveform of Mesh topology

### D. RING 8 PORT SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Router on Ring Topology. Here fig.. show the 8 port Router for Ring topology simulated waveform


Figure 6: shows the simulated waveform of a Ring topology

### E. STAR 8 PORT SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Routers on Star Topology. Here fig. show the 8 port Router for Star topology simulated waveform


Figure 7: shows the simulated waveform of a Star topology

### F. TORUS 8 PORT SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Router on Torus Topology. Here figure show the 8 port Router for Torus topology simulated waveform.

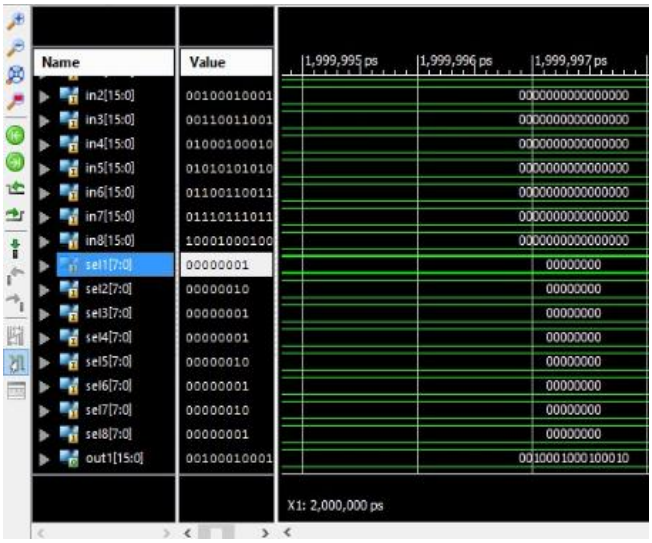


Figure 8: shows the simulated waveform of Torus topology

### G. FAT TREE 8 PORT SIMULATED WAVEFORM

The results attained based on the evaluation methodology that was set for designing the 8 Port Router on Fat tree Topology. Here fig. show the 8 port Router for Fat tree topology simulated waveform

 


Figure 9: shows the simulated waveform of Fat Tree topology

## V. COMPARATIVE STUDY

Table 1: Comparative study of 8port NoC Router for different topologies on the basis of power consumptions

| Serial no. | | Octagon topology | Mesh topology | Ring topology | Star topology | Torus topology | Fat tree topology |
|---|---|---|---|---|---|---|---|
| 1. Logic | | | | | | | |
| | used | 272 | 493 | 136 | 82 | 345 | 53 |
| | available | 69120 | 69120 | 69120 | 69120 | 69120 | 69120 |
| | utilization | 0% | 1% | 0% | 0% | 0% | 0% |
| 2. Signal | | | | | | | |
| | used | 481 | 645 | 328 | 338 | 481 | 53 |
| | available | --- | --- | --- | --- | --- | |
| | utilization | --- | --- | --- | --- | --- | |
| 3. IOs | | | | | | | |
| | used | 321 | 273 | 321 | 273 | 321 | 209 |
| | available | 640 | 640 | 640 | 640 | 640 | 640 |
| | utilization | 50 | 43 | 50 | 43 | 50 | 33 |
| 4. Clock power | | 0.009 | 0.010 | 0.008 | 0.001 | 0.007 | 0.003 |
| 5. Leakage power | | 1.186 | 1.186 | 1.186 | 1.186 | 1.186 | 1.186 |
| 6. Total power | | 1.195 | 1.196 | 1.194 | 1.188 | 1.194 | 1.189 |
| 7. Thermal properties | | | | | | | |
| • effective TJA | | 1.4 c/w | 1.4 c/w | 1.4c/w | 1.4c/w | 1.4c/w | 1.4c/w |
| • Max ambient | | 83.3c | 83.3 c | 83.3c | 83.4c | 83.3c | 83.3c |
| • Junction Temp | | 51.7c | 51.7 c | 51.7c | 51.6c | 51.7c | 51.6c |
| 8.Supply Power | | | | | | | |
| • Total | | 1.195w | 1.196w | 1.194w | 1.188w | 1.194w | 1.189w |
| • Dynamic | | 0.009 w | 0.010w | 0.008w | 0.001w | 0.007w | 0.003w |
| • Quiescent | | 1.186w | 1.186w | 1.186w | 1.186w | 1.186w | 1.186w |

## VI. CONCLUSION

The NoC area has a significant influence in the design of next-generation SoC or multicore architectures. An 8port router is designed and synthesized in Verilog using Xilinx 14.3 software for NoC with Octagon, Mesh, Ring, Star, Torus and Fat tree topology. A comparative study is made between the six router designs based on the device utilization and power analyzer of the router. The values of thermal properties for 8 port router of Octagon, Mesh, Ring, Torus and Fat tree are same except star topology and supply

 

power are independent of router's topology. it is observed that design of 8 port routers of Octagon, Mesh, Ring, Star, Torus, Fat tree are having same leakage power is 1.186w. The total power consumed for Octagon is 1.195w, Mesh is 1.196w, Ring is 1.94w, Star is 1.88w, Torus is 1.194w and a Fat tree is 1.189w. Utilization is maximums for 8 port router for of Octagon, Mesh, Ring and Torus and more increase its logic, signal, and IOs is increased but Star topology is less as compared. Future work can be done for implementation of different topologies by designing suitable efficient router architecture and verification using improved methodology.

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## REFERENCES

[1] M. Palesi, R.Holsmark, S. Kumar, and V. Catania, "Application-specific routing algorithms for a network on chip," IEEE Transactions on Parallel and Distributed Systems, vol. 20, no3 pp. 316-339, 2009

[2] L. Benini and D. Micheli, Networks on Chips: A New SoC Paradigm, IEEE Computer, vol.35 pp.70-78(2002).

[3] V. Dumitriu and G. N. Khan, "Throughput- oriented NOC topology generation and analysis for high-performance SOC," IEEE Transactions on VLSI Systems, vol. in press 2009.

[4] A. Chien, "A cost and speed model for k-ary n-Cube Wormhole Routers," IEEE Transactions on Parallel and Distributed Systems, vol.9, no2, pp.29-36, Feb 1998.

[5] B. H. Meyer, J.J. Pieper, J.M. Paul, J.E. Nelson, S. M. Pieper and A.G.Rowe, "Power-performance simulation and design strategies for single-chip heterogeneous multiprocessors," IEEE transactions on Computers, vol.54, no. 6, pp.684-697, Jun 2005.

[6] L. S. Peh and W. J. Dalley, A delay model for router microarchitectures," IEEE Micro, vol.21, no. 1, pp. 26-34, Jan. 2001.

[7] T. Bjerregaard and K. Mahadevan, "A survey of research and practices of network-on-chip,"ACM Computing Surveys, vol. 38, pp.38, pp.1-51, Mar. 2006.

[8] V. Pavlidis and E. Friedman," Interconnect-based design methodologies for three-dimensional integrated circuits'' Proceeding of the IEEE, vol.97, no.1, pp.123-140, 2009.

[9] H. Elmiligi, A. Morgan, M. W. EI-Kharashi, and F. Gebli, " Power Aware Topology Optimization for Network-on-chips," in a proceeding of the IEEE International Symposium on Circuits and SystemsConference on Design and Test of Integrated Systems in Nanoscale Technology, Era Cario, Egypt, Apr. 6-9, 2009, pp.107-112.

[10] Axel Jantsch and Hannu Tenhunen(Eds.), Networks on a chip, Kluwer Academic Publishers, 2003

[11] A Delay-Aware Topology-based Design for Network-on-chip Applications By Haytham Elmiligi, Ahmed A. Morgan, M. Watheq El-Kharashi, Fayez Gebali.IEEE transaction, 2009.

[12] Khalid Latif, Tiberiu Seceleanu, Hannu Tenhunen, "Power and Area Efficient Design of Network-on-Chip Router Through Utilization of Idle Buffers", In the proceedings of the 2010 17th IEEE International Conference and Workshops on Engineering of Computer Based Systems.

[13] Cheng Liu·, Liyi Xiao, Fangfa Fu, Design and "Analysis of On-Chip Router", IJCTT, Aug 2011

[14] W. Zhou, Y. Zhang, and Z. Mao," An application specific NOC mapping for the optimized delay," in a proceeding of the IEEE International Conference on Design and Test of Integrated Systems in Nanoscale Technology, Tunis, Tunisia , Sept. 5-7, 2006, pp. 184-188.

[15] M. Nickray, M.Dehyadgari, and A. Afzali-kusha, "Power and Delay optimization for a network on chip," in Proceedings of the 2005 European Conference on Circuit Theory and Designs, Cork, Ireland, Aug-28-2 Sept. 2005, pp. 273-276.

[16] H. Elmiligi, A. A. Morgan, M. W. EI-Kharashi and F. Gebli, " A reliability-aware design methodology for network-on-chip applications," in proceeding of the IEEE International Conference on Design and Test of Integrated Systems in Nano scale Technology ,Era Cario, Egypt, Apr. 6-9, 2009, pp. 107-112.

[17] M. Mirza-Aghatabar+,S.Koohi+, S. Hessabi*, M. Pedram†," An Empirical Investigation of Mesh and Torus NoC Topologies Under Different Routing Algorithms and Traffic Models", IEEE International Conference on Digital System DSD 2007.

[18] Victor Dumitriu and Gul N. Khan, "Throughput-Oriented NoC Topology Generation and Analysis for High-Performance SoCs", IEEE transactions on very large scale integration (vlsi) systems, vol. 17, no. 10, october 2009.

[19] Mahmoud Moadeli1, Ali Shahrabi2, Wim Vanderbauwhede1, Mohamed Ould-Khaoua1," An Analytical Performance Model for the Spidergon NoC", IEEE 21st International Conference on Advanced Networking and Applications (AINA'07) 2007.

[20] Ville Rantala, Teijo Lehtonen, Juha Plosila, 'Network on Chip Routing Algorithms," Journal of Systems Architecture, TUCS Technical Report No 779, pp. 5-7, August 2006

[21] K.Shiney, .K.V.Subrahmanyam and S Chandra Sekhar "High throughput compact delay-insensitive asynchronous NoC router" IJCSE, October 2014

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