IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.-7, Issue-3, March 2019 E-ISSN: 2347-2693

Power Efficient Multi-Stage Decimation Filter for Wideband Sigma-Delta ADCs

N.N. Hurrah[1*], S.A. Parah[2], N.A. Loan[3]

[1,2,3] Department of Electronics and Inst. Technology, University of Kashmir, Srinagar, J&K, India

[*]*Corresponding Author: hurrah.scholar@gmail.com, Tel.: +91-7006297913*

DOI: https://doi.org/10.26438/ijcse/v7i3.800806 | Available online at: www.ijcseonline.org

Accepted: 08/Mar/2019, Published: 31/Mar/2019

***Abstract*—** The problems while designing a communication module comes up during hardware implementation in terms of power, area and speed. This paper presents an efficient decimation filter optimized in terms of power and area for wideband Sigma-Delta (ΣΔ) A/D converters. A work flow for a rapid design of this optimized decimation filter in MATLAB, along with its implementation is presented. The design is suited particularly for filters with high decimation factor. The filter offers a decimation factor of 128 having input of 3 bits from over-sampled ΣΔ modulator. The ΣΔ modulator having an input of 0.8MHz and sampling rate of 208MHz provides oversampling by a factor of 128 and resolution of 12 bits. Techniques like transposed direct-form polyphase decomposition, pipelining, retiming, resource sharing and CSD encoding are used for efficient design. The filter offers reduced power consumption and thereby suited for multi-rate filter design in state of art Sigma-Delta Analog to Digital converters.

***Keywords*—**Sigma Delta, ADC, Decimation filter, CSD, Multi-rate filter.

I. INTRODUCTION

With the need of hand-held and portable personal communication systems growing day by day the design of small size, low power and high performance devices is also growing [1]. Therefore, it is required to have an efficient, reliable and flexible signal processing. Moreover, due to the fast progress and rapid scaling of CMOS technology, digital signal processing (DSP) systems have almost replaced analog ones. Analog to digital converter (ADC) forms an important section of a signal processing system and it may be a continuous or a discrete type. Currently an efficient choice for data converters is an oversampling ADC due to its small silicon area, low power consumption and higher resolution unlike traditional ones having Nyquist frequency limit [2]. The oversampling ADCs sample analog signal with higher sampling rate than Nyquist rate, which is usually expressed through oversampling ratio (OSR). Also, particularly they are favored for high speed applications as they are relatively simple and possess resistance against component mismatch and circuit errors.

Compared to traditional data converters, perhaps one of most important advantage among various others is their ease of implementation on a high-speed single chip VLSI circuit. Broad understanding of data converters can be obtained in [3,4,5,6] and references therein. Presently ΣΔ ADCs are the best converters used for implementation in nm CMOS technology. The applications of ΣΔ ADCs are increasing day by day in different areas like wideband applications (SDR, LTE etc), medical and audio applications. Several papers that deal with different implementation architectures of decimation filter architecture in case of ΣΔ ADCs are available in literature.

As FIR filters are extremely stable and possess linear phase characteristics they are widely used in DSP applications [7, 8]. Therefore, in the research community significant attention has been given to the optimized implementation of finite impulse response (FIR) filters in hardware. Also there exist several issues while designing and implementing a digital filter like area, power consumption, and magnitude and frequency response. Usually power consumption in a circuit is reduced by decreasing either of operating voltage or clock rate. But in case of ΣΔ ADCs the power consumption will increase as it utilizes oversampling at high clock rates. Also circuit delay increases on lowering the operating voltage which clearly will put a limit on operating frequency. Different solutions were proposed from time to time among which one is parallel processing. Traditionally, in signal processing parallel structures have been implemented by polyphase decomposition [9]. As such DSP functions are usually implemented on dedicated DSP processors or Application Specific Integrated Circuit (ASICs). While as DSP processors are flexible and less expensive but offer low speed for operation, ASICs have high speed but have cost

and flexibility problem. So an alternative approach is provided in the form of Field Programmable Gate Arrays (FPGAs) as such they offer all above advantages and remove problems [10]. Also as FPGA architectures offer system programmability the functionality of the device can be modified as per the need.

Several papers have proposed methods to reduce power consumption but at the expense of increased area [11, 12, 13, 14]. Others have used only recursive filter algorithms at initial stages of decimation filter [15, 16, 17, 18]. This work seeks to better the factors that like power consumption speed of operation along with the minimum possible area utilization while implementing complete decimation filter. The use of HBF's and conventional FIR filters ensure that stopband and passband response did not get affected. In this paper we discuss the design and implementation of low power high speed decimation filter using non-recursive as well as recursive filter algorithms and the designs are compared. Keeping in mind that there have been several factors reported that effect the performance of a multistage filter design, there is need to keep them in a range desirable for an optimal design. For example, it has been shown that the total number of stages and their rate changing factors have considerable effect on filter latency and area while as memory usage, computational cost and their realization methods affect the power consumption [19]. So there is a demandable research work needed to design a model that considers the mentioned aspects for optimal multistage design.

The starting point in this work is the ΣΔ modulator and decimation filter specification. According to these specifications model of ΣΔ modulator is designed in the Matlab with the techniques fulfilling these specifications. The Matlab model and the architecture are designed and modified simultaneously if needed, to meet the correct functionality. The filter model created in Matlab is then translated into HDL code required for implementation of the design. The filter is then implemented in using this code in the Xilinx platform. Finally, this HDL model is synthesized successfully in Xilinx. It should state the purpose and summarize the rationale for the study and gives a concise background.

Rest of the paper is organized as follows, Section I contains the introduction about the proposed technique. Section II contains the discussion about prelimanaries. Section III contains the methodology about the proposed design. Section IV describes results and discussion and Section VIII concludes research work with future directions.

II. PRELIMANARIES

A detailed explanation on the theory and fundamentals for ΣΔ modulators is given in [2, 4] and references therein. Next, a basic overview of ΣΔ converters and decimation filter is presented.

A. Sigma Delta Analog to Digital Converters

As well known, ΣΔ converters are made up of mainly two blocks:

- Modulator: where the signal is oversampled and quantization noise shaping takes place and
- Decimator: whose function is to decrease the frequency of the output from the oversampled modulator up to the Nyquist rate. Another function of the decimation filter is to keep the passband aliasing within the prescribed limits.

Oversampling data converters have gained a lot of popularity the last two decades. Block diagram of an oversampling ΣΔ ADC shown in Fig. 1, has two main parts i.e. sigma delta modulator (ΣΔM) followed by decimator, where Fs is the sampling frequency and N is the decimation factor. In addition, it also includes an Anti-Aliasing Filter (AAF). This AAF preceding the ΣΔM reduces the aliasing back (due to oversampling) effect of out-of-band noise [7].

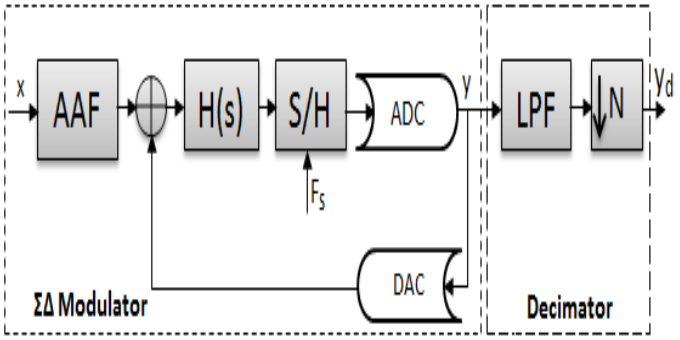

Figure 1. ΣΔ ADC block diagram

In ΣΔM, signal is oversampled and quantization error is shaped and pushed to higher frequencies of stop band. Therefore, outside signal band most of the power of quantization noise is present which can be easily filtered out by a digital filter following ΣΔM. The modulator includes of a loop filter (integrator) in forward path i.e. H (s), single or multi-bit quantizer, and a DAC in feedback path. The decimator includes a decimation filter followed by a down sampler.

B. Decimation Filter Design

A decimator has the function to decrease the frequency of the output from the oversampled modulator up to the Nyquist

rate. Decimation is performed by an integer factor by removing the samples from a sequence until the required sampling rate is obtained. Another function of the decimation filter is to keep the passband aliasing within the prescribed limits. Usually the input signal to the decimator is band limited in order to avoid aliasing after decimation. This is done by a low pass anti-aliasing filter before the removing of samples. A decimation structure, including the anti-aliasing filter and the sample removal, is shown in Fig. 2.

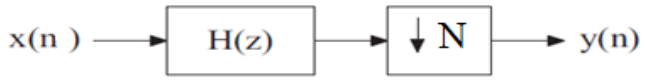

Figure 2. Decimation filter

There are several architectural options available for implementing a decimation filter:

III. METHODOLOGY

The proposed filter is a wideband decimation filter for 0.7-10 MHz to be used in wideband Delta-Sigma ADCs for application like LTE. The designed decimation filter is a low power high speed filter with the decimation ratio of 128 which can be programmed easily as per need by choosing different sampling rates for different input signal bandwidth. The decimation filter consists of two non-recursive comb filter, a CIC filter, two half band filters and a FIR filter. The polyphase decomposition technique is also used to minimize the power consumption further. Matlab Simulink with ΣΔ toolbox from SIMSIDES is being used for simulation with ΣΔM designed by SIMSIDES toolbox [24]. The decimation filter is implemented using Xilinx design suite and power is calculated using its XPower Analyzer.

Table 1. Specifications of Modulator and Decimation Filter

Modulator		Decimation filter	
Order	3	***Input no. of bits***	3 bits
Bandwidth	0.8 MHz	***Output no. of bits***	12 bits
OSR	128	***Decimation factor***	128
Sampling frequency	208 MHz	***Output rate***	0.8 MHz

The decimation filter comprises of decimation by- 2 non recursive input stages followed by decimation by 4 Sinc stage. The multistage architecture offers the advantage that most of the filter hardware can operate at a lower clock frequency, and thus hardware complexity gets reduced as compared to a single state decimator. In order to filter and suppress majority of the quantization noise initially three comb filters are used which also provide a clock rate decimation factor of 16. Also a higher decimation factor should be avoided in first stage as it results in drastic power consumption.

After the comb filters a second type of filter follows, called half band filter (HBF), is used which provides a sharp passband to stop band transition and decimation factor of 2. To achieve the droop compensation an introduced by the comb stages an FIR equalizer is used. The complete designed decimator block diagram is shown in Fig. 3.

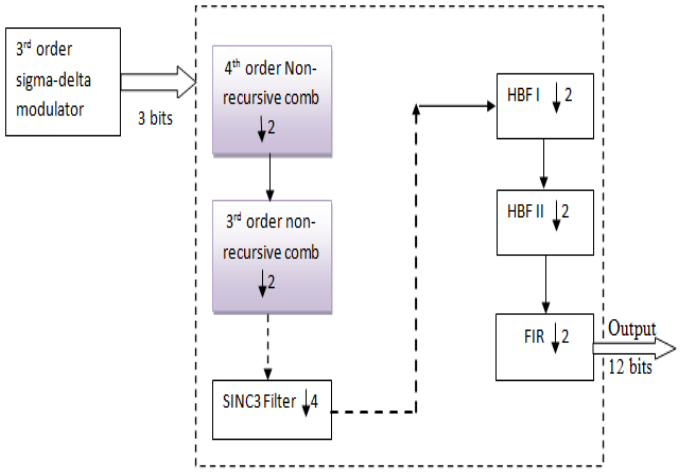

Figure 3. Proposed architecture of decimation filter

Various techniques have been used to optimize the custom designed decimation filters. These techniques include multi-rate filtering, pipelining, retiming [25**]**, resource sharing and employing power efficient number systems e.g. canonical signed digits (CSD). Similarly, during the synthesis of digital logic there is need of various optimizations. All sub-filters of the decimation filter are described in detail in the following sections.

A. Non-recursive comb filters (1st and 2nd stage)

The first two stages of the decimation filter designed are non-recursive filters with first one of 4th order and second of 3rd order respectively keeping in mind the compatibility issues and decimation factor requirements. The non-recursive filters are used due to the low power consumption and ability to increase the circuit speed [26]. It is usually required that for a Kth-order modulator the order of the anti-alias filter should be one up in order for meeting the anti-aliasing requirements [2]. As the noise shaping order of the ΣΔM is taken to be 3 in the design so the 4th order first stage non-recursive filter is used for better performance and anti-aliasing characteristics. This first stage operates at the rate of oversampling obtained from the oversampling modulator. Input stage of the design is very important due to the fact that it can result in large power dissipation as being working at the highest clock

frequency that is why only decimation by 2 stages are used [27].

As described earlier that for the 3rd order modulator a 4th order filter is used for better performance.

$$M_1(z) = (1 + z\text{-}1)^4 = 1 + 6z^{-2} + z^{-4} + z^{-1}(4 + 4z^{-2})$$
$$= F_0(z) + z^{-1}.\, F_1(z) \quad (1)$$

This expression implemented using polyphase decomposition structure is shown in Fig. 4.

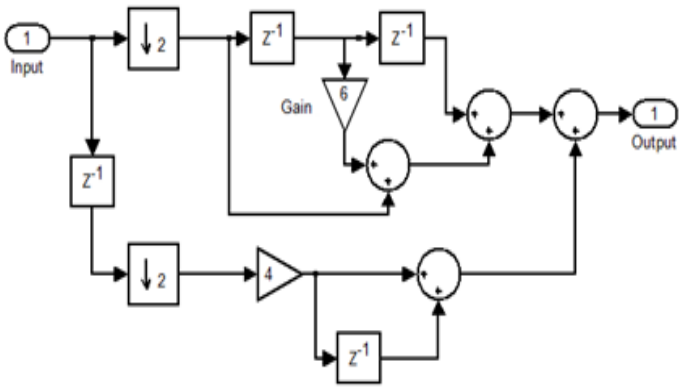

Figure 4. $H_1(z)$ (sub-filter) implementation

First stage is followed by 3rd order non-recursive filter derived from following expression:

$$M_2(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^{-3}$$
$$= 1 + 3z^{-1} + z^{-1}(3 + z^{-2})$$
$$= F_0(z) + z^{-1}.\, F_1(z) \quad (2)$$

This expression implemented using polyphase decomposition structure is shown in Fig. 5.

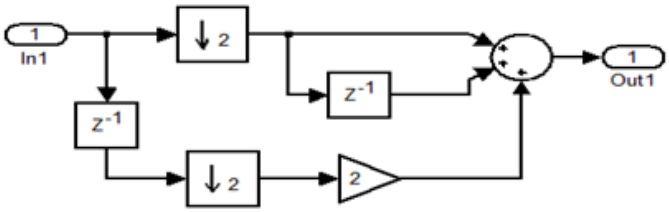

Figure 5. $H_2(z)$ (sub-filter) implementation

These filters are best choice for initial filtering in order to suppress most of the noise introduced by the quantization in the modulator. The word-lengths of the two stages are calculated as per the expression:

$$Bout = K + Bin \quad (3)$$

Where k is the order of the non-recursive filter and Bin is the word-length of the input to the filter. Both these filtering stages are implemented using polyphase decomposition technique.

B. CIC or Sinc Filter (3rd stage)

The Sinc filter forms the third stage of the decimation filter and is used for further suppression of the quantization noise. This filter is used after the non-recursive filters in order to meet the area constraints of the decimation filter because Sinc filter is an area efficient filter due to the absence of the multipliers and storages.

In the proposed decimation filter the 3rd order Sinc filter performing decimation of 4 is used. If the differential delay D=1 then its transfer function is

$$M_3(x) = \left(\frac{1-x^{-4}}{1-x^{-1}}\right)^3 \quad (4)$$

which can be solved as

$$M_3(x) = (1+x^{-1})^3\,(1+x^{-2})^3 = (1+x^{-1}+x^{-2}+x^{-3})^3 \quad (5)$$

The polyphase decomposition technique used removes the critical path problem present in the CIC filter architecture and thus increases the speed of operation of the design. Adding to it, only first three registers having small internal word-length operate at higher sampling frequency than others proceeding after down sampler. Thus we can eliminate or share many items implemented through x^{-4} resulting in reduced power consumption. Hence we can get for polyphase implementation

$$M_3(x) = F_0(x) + x^{-1}F_1(x) + x^{-2}F_2(x) + x^{-3}F_3(x) \quad (6)$$

where

$$F_0(x) = 1 + 12x^{-1} + 3x^{-2} \quad (7)$$

$$F_1(x) = 3 + 12x^{-1} + x^{-8} \quad (8)$$

$$F_2(x) = 6 + 10x^{-1} \quad (9)$$

$$F_3(x) = 10 + 6x^{-1} \quad (10)$$

This expression is implemented using polyphase decomposition structure using adders, gain elements, etc. as done for eq. 1 and eq. 2 in Fig. 4 and Fig. 5.

C. Half Band Filters (HBFS)

The use of comb filters which are simple in structure have largely reduced the rate of sampling. However, the stopband attenuation achieved is not sufficient to meet the desired application demands. Therefore, a cascaded combination of two FIR HBFs is used to further increase the stopband attenuation [28]. In this paper, the HBF is implemented with a direct form transposed FIR polyphase decimator structure to reduce power consumption and hardware complexity [5]. The output sampling rate (13MHz) of the 3rd order CIC filter is same as the input sampling rate of the first HBF. Due to down-sampling the output sampling rate of the first half-band FIR filter stage is 6.5MHz. This HBF can be implemented by using a filter of low order whose transition band is relatively wide. Specifications of first HBF are shown in Table 2.

Table 2. Specifications of first HBF

Filter type	FIR
Response Type	Low pass
Filter type	Decimator
Stopband attenuation	65dB
Design method	Equiripple

Like 4th stage the 5th stage used in the design is the computationally efficient HBF. Their efficiency lies in the fact that they have approximately half of the coefficients equal to zero implying that large amount of computing power can be saved. Other characteristic of HBFs is that they have equivalent passband and stopband ripples and symmetrical passband and stopband frequencies around Fs/4 of sampling frequency. Due to these advantages they are used as the 4th and 5th stage of the decimation filter design. The 4th stage HBF used in the design is of 6th order. While the 5th stage HBF is of 14th order. The HBFs suppress the initial quantization noise the will relax the requirements for the preceding FIR filter. Both of HBFs use the direct form transposed FIR polyphase decimator structure configuration

D. FIR Lowpass Filter

The last stage of the decimation filter is a 36th order decimation filter. It is a LPF which performs down-sampling by a factor of 2. Like HBFs FIR filter is designed and realized using the "Filter-builder" option in the MATLAB and its HDL code is generated using HDL Coder Toolbox therein. For the HDL code generation CSD format is used to encode the tap coefficients of the HBFs in order to technique in order to increase speed of operation and reduce the computation power.

Table 4 Specifications of FIR filter

Type	**Low pass**
Order	36
Stopband attenuation	60dB
Sampling frequency	3.25MHz
Design method	Equiripple
Phase constraint	Linear
Passband frequency(Normalized)	0.45
Stopband Frequency(Normalized)	0.55

IV. RESULTS AND DISCUSSION

The work done in this paper is to design a SD ADC for wideband applications with special focus on the design and implementation of decimation filter part. Design and simulation is done for whole ADC and implementation is only done for decimation section of the converter.

A. Simulation Setup

The two main sections of the ADC are CT ΣΔ modulator and Decimation Filter. The modulator used in the design is the CT ΣΔ modulator which is designed using "SIMSIDES" Toolbox in the Simulink environment [24]. The decimation filter is also designed in the Simulink environment of MATLAB. The complete setup is shown in Fig. 3.

B. Implementation

Keeping in view the various area and power considerations proposed in literature a complete filter has been implemented [30, 6]. The decimation filter was synthesized using precision synthesis tool and the top view of resulting RTL schematic is shown in Fig. 6. To implement this structure, we used FPGA Family: Artix-7; Device: XC7A100T; package: CSG324, which provides a user advantages like low power dissipation, high density packaging and high yield.

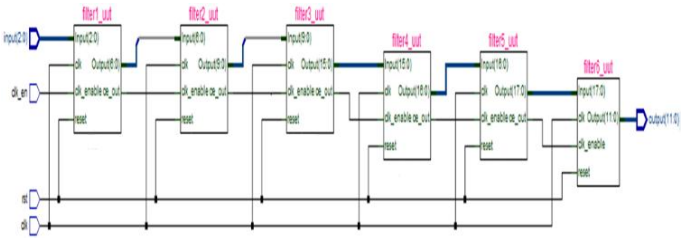

Figure 6. RTL Schematic of proposed filter in Precision Tool

C. Power consumption

The power consumption of the decimation filter is calculated after implementation in Xilinx through XPower Analyzer tool provided by Xilinx. The power calculation has been done for Artix 7 [29].

Table 6. Comparison of Dynamic Power Consumption

Dynamic Power Consumption(mW)		
Type	***Architecture with recursive input stages***	***Proposed optimized architecture***
Logic	0.17	0.02
Data Signals	0.23	0.03
Clock Enable Signals	0.16	0.04
Set/Reset Signals	0.04	0.03
I/Os	1.02	0.36
Clock Domain	10.52	8.4
Total	**12**	**9**

V. CONCLUSION AND FUTURE SCOPE

The work in this article focused on the designing of the low power decimation filter by modifying the already present architectures with different approaches and techniques. The proposed filter has been targeted for wideband applications. The algorithms and the filter structures chosen are hardware realizable in which low power is the most important constraint. The suitable low power techniques are applied in each case to minimize power consumption of the device targeted. The designed filter was targeted for being implemented in FPGA kit. The designed and implemented digital decimation filter consists of six stages (Comb-HBF-FIR) for high-resolution delta-sigma applications. It has been shown that use of non-recursive comb filter results in reduction in word-lengths as achieved by proposed architecture and thereby reduces power consumption and increases speed of operation.

ACKNOWLEDGMENT

This publication is an outcome of the R&D work undertaken project under the Visvesvaraya PhD Scheme of Ministry of Electronics & Information Technology, Government of India, being implemented by Digital India Corporation.

REFERENCES

[1] Anjum Mohd Aslam, Mantripatjit kaur, "A Review on Energy Efficient techniques in Green cloud: Open Research Challenges and Issues", International Journal of Scientific Research in Computer Science and Engineering, Vol.6, Issue.3, pp.44-50, 2018.

[2] Candy J. C., Temes G. C., "Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation", IEEE Press, 1992.

[3] J.M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State- of-the-Art Survey", IEEE Trans. on Circuits and Systems I: Regular Papers. Vol. 58, pp. 1-21, 2011.

[4] Schreier R., Temes G. C., 2005. Understanding Delta-Sigma Data Converters New York: IEEE Press.

[5] Norsworthy S. R., Crochiere R. E., 1997. Decimation and interpolation for sigma delta conversion. in Delta Sigma Data Converters. Piscataway, NJ: IEEE Press.

[6] N. N. Hurrah, Z. Jan, A. Bhardwaj, S. A. Parah, A. K. Pandit, 2015. Oversampled Sigma Delta ADC Decimation Filter: Design Techniques, Challenges, Tradeoffs and Optimization. Proc. of RAECS UIET Panjab University Chandigarh.

[7] Proakis J. G., Manolakis D. G., 2007. Digital Signal Processing, Pearson Prentice Hall.

[8] Shuni Chu, Burrus C. S., 1984. Multirate Filter Designs Using Comb Filters. IEEE Trans. on Circuits and Systems. 31(11).

[9] Uwe Meyer-Baese. Digital Signal Processing with Field Programmable Gate Arrays. 3rd Edition, Springer.

[10] Chandan Singh, "Realization of FIR Filter using Distributed Arithmetic Architecture", International Journal of Scientific Research in Computer Science and Engineering, Vol.3, Issue.4, pp.7-12, 2015

[11] Ahmed, N.Y., Ashour M. A., Nassar, A.M., 2008. Power Efficient Polyphase Decomposition Comb Decimation Filter in Multi-Rate Telecommunication Receivers. IEEE, Mosharaka International Conference, pp. 1-6.

[12] Noha Younis, Mahmoud Ashour, Amin Nassar, 2009. Power-Efficient Clock/Data Distribution Technique for Polyphase Comb Filter in Digital Receivers. IEEE Trans. on circuits and systems—II: Express Briefs, 56(8).

[13] Abbas, M., Gustafsson, O., Wanhammar, L., 2010. Power Estimation of Recursive and Non-Recursive CIC Filters Implemented in Deep-Submicron Technology. IEEE Int. Conf. Green Circuits Syst., Shanghai, China, June 21-23.

[14] Salgado, G. M., Dolecek, G. J., de la Rosa, J.M., 2013. Power and area efficient comb-based decimator for sigma-delta ADCs with high decimation factors. Proc. of the IEEE International Symposium on Circuits and Systems, pp. 1260-1263.

[15] Yi Xie, Minglei Zhang, Baoyue Wei, Xiaohua Fan, 2014. High-Speed Low-Power Decimation Filter for Wideband Delta-Sigma ADC. Proc. Of IEEE 57th International Midwest Symposium on circuits and systems. pp. 591 – 594.

[16] Xiong Liu, 2009. A High Speed Digital Decimation Filter with Parallel Cascaded Integrator-Comb Pre-filters. IEEE.

[17] Alp Kilic, D. Haghighitalab, H. Mehrez, Hassan Aboushady, 2014. Low-Power Comb Decimation Filter for RF Sigma-Delta ADCs. Proc. of IEEE International Symposium on Circuits and Systems, pp. 1596 – 1599.

[18] Mohan, R., Koppula, R., Balagopal, S., Saxena, V., 2011. Efficient design and synthesis of decimation filters for wideband Delta-Sigma ADCs. SOC Conference (SOCC), IEEE International, Taipei, pp. 380 – 385.

[19] Zhu, X., Wang, Y., Hu, W. and Reiss, J.D., 2016. Practical considerations on optimising multistage decimation and interpolation processes. In Digital Signal Processing (DSP), 2016 IEEE International Conference on (pp. 370-374). IEEE.

[20] B. B. Hogenauer, 1981. An economical class of digital filters for decimation and interpolation. IEEE Trans. on Acoustics, Speech and Signal processing. 29(2). 155-162.

[21] Aboushady, H., Dumonteix, Y., Louërat, M., Mehrez, H., 2001. Efficient Polyphase Decomposition of Comb Decimation Filters in ΣΔ Analogto-Digital Converters. IEEE Transactions on Circuits and Systems II. 48(10), 898-903.

[22] Shahana, T. K., James, R. K., Jose, B. R., Jacob, K. P., Sasi, S., 2007. Polyphase Implementation of Non-recursive Comb Decimators for Sigma-Delta A/D Converters. Electron Devices and Solid-State Circuits, IEEE Conference, Tainan, pp. 825–828.

[23] Yeung K. S. and Chan S. C., 2004. The design and multiplier-less realization of software radio receivers with reduced system delay. IEEE Trans. Circuits Syst. I, Reg. Papers. 51(12), 2444–2459.

[24] J.M. de la Rosa, Rocio del Rio, 2013. Cmos Sigma-Delta Converters Practical Design GUIDE. first edition, John Wiley & Sons.

[25] Fischer, R., Buchenrieder, K. and Nageldinger, U., 2005. Reducing the power consumption of FPGAs through retiming. In Engineering of Computer-Based Systems. ECBS'05. 12th IEEE International Conference and Workshops on the, pp. 89-94.

[26] Bibin John, Fabian Wagner, Wolfgang H. Krautschneider, 2005. Comparison of Decimation Filter Architectures for a Sigma-Delta Analog to Digital Converter. Institute of Nanoelectronics Hamburg University of Technology (TUHH).

[27] Salgado, G.M., Dolecek, G.J. and Jose, M., 2016. Low power two-stage comb decimation structures for high decimation factors. Analog Integrated Circuits and Signal Processing, vol. 88, no. 2, 245-254.

[28] Vaidyanathan, P., Nguyen, T., 1987. A TRICK for the design of FIR halfband filters. IEEE Trans. Circuits Syst., vol. 34, 297-300.

[29] Ian Beavers, 2015. Rethinking Digital Down conversion in Fast, Wideband ADCs. Xcell Journal, spring.

[30] Dolecek, G.J., Baez, J.R.G. and Laddomada, M., 2017. Design of Efficient Multiplierless Modified Cosine-Based Comb Decimation

Filters: Analysis and Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers. vol. 64, no. 5, 1051-1063.

Authors Profile

Mr Nasir N. Hurrah pursed Bachelor of Science and Master of Science from University of Kashmir, India in year 2009 and 2012 respectively. He is currently pursuing Ph.D. in Department of Electronics, University of Kashmir, since 2015. He is a member of IEEE & IEEE Microwave Society since 2016. He has published more than 10 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE and it's also available online. His main research work focuses on Digital Filter Design for Signal Processing and Communications, Cryptography Algorithms, Network Security, Cloud Security and Privacy, Image Processing, Watermarking, IoT and VLSI Design. He has 6 years of Research Experience. He is pursuing Ph. D under VISVESVARAYA PHD Scheme for Electronics and I.T., sponsored by Ministry of Electronics & Information Technology Government of India.

Shabir A. Parah has completed his M. Sc. and M. Phil and Ph.D. in Electronics from University of Kashmir, Srinagar in the year 2004, 2010 and 2013 respectively in the field of Signal processing and Data hiding. He is working as Assistant Professor in the department of Electronics and I. T, University of Kashmir, Srinagar. His fields of interest are Multimedia Signal Processing, Secure Communication, Digital Watermarking and Steganography. Dr. Shabir A. Parah has guided about twenty-five PG projects. He has published more than 100 research papers in International/National journals and conference proceedings.

Nazir A. Loan is a doctoral scholar in the Department of Electronics and IT, University of Kashmir and is currently working on the Development of Robust watermarking algorithms for multimedia applications. He is INSPIRE fellow of Department of Science and Technology Government of India.

