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Energy Efficiency of Microprocessor

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Abstract— In the microprocessor industry we see that energy efficiency is one-off the main issues that we are faced with. The motivation for our paper is the increased applications which use embedded systems for communication and multimedia. In our paper you will see the changes in techniques that have made a considerable amount of development to make sure that the efficiency of the microprocessor consumes will be less but also not compromise with the performance (clock speed) that it provides to the users. Internet connectivity has caused the devices to be in use all day long because of this the rate at which the microprocessor runs uses great amount of energy because of which energy efficiency has to be good. Ever since caches were introduced they present the most attractive ways for power reduction. To implement coherent caches using MESI protocol we use snoop filtering mechanism.

Keywords—Energy, CMOS, Cache, Snoop Filtering.

I. INTRODUCTION

The recent years have witnessed the emergence of multicore microprocessor chips (CMPs) as a practical and expedited way of exploiting the potentials of increasing number of transistors within a chip to make it energy efficient, thus improve performance, most microprocessors have one or two levels of on-chip caches. An energy-efficient design methodology has been developed for signal processing applications, resulting in a strategy to provide orders of magnitude of power reduction. For the chips, the cache power consumption is either the large or second largest power-consuming block. These trends will probably continue as embedded processors become more sophisticated and provide higher performance.

A framework for an energy-efficient design methodology more suitable for a microprocessor's two operating modes will be presented:

1. Maximum throughput
2. User interactive mode

Using simple analytic models for delay and power in CMOS circuits, metrics of energy efficiency for the above modes of operation will be developed.

Energy efficiency:

$$\text{Throughput} \equiv T = \frac{operations}{second} \alpha \frac{\text{concurrency}}{Delay}$$

The figure shows the basic filter cache organization as compared to the traditional memory organization. The main memory only consumes power for the bus capacitance and the power consumed by the memory chip.

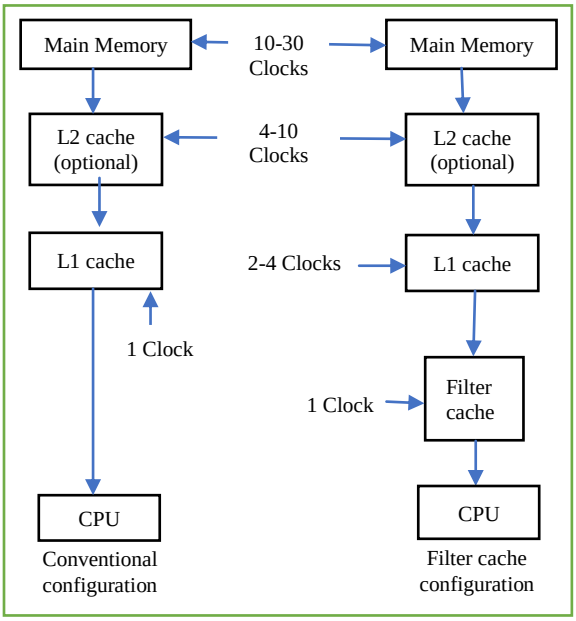

Fig: 1. Power and Performance characteristics of traditional caches and the filter cache

II. RELATED WORK

In [1] this paper we have examined that the CMOS circuits have both static and dynamic power dissipation. To reduce power dissipation in CMOS microprocessor we need to qualify three important design principles for energy efficient microprocessor design. A high-performance processor is usually an energy-efficient processor: reducing the clock frequency does not increase the energy efficiency; and lastly, idle power dissipation limits the efficient of increasing deliverable throughput. By identifying the major modes of computation of these processors, a power analysis methodology is developed and it also allows the energy efficiency of various CMOS architectures to be quantified.

In [2] this paper we explored that Caches clearly present one of the most attractive targets for power reduction. Modern microprocessors employ one or more levels of on-chip cache in order to improve performance. The power decrease in the cache can be achieved by many ways: 1. semiconductor process improvements, 2. memory cell redesign, 3. voltage reduction and 4. Optimized cache structures. Caches often use a significant amount of power. In applications, such as portable devices, as we have seen that low power is more important than performance .It was propose to trade performance by making the L1 cache unusually small for power consumption. Several techniques have been discovered which lead to an increased performance as well as reduced power consumption.

In [3] this paper we studied that the In this paper we have seen that recent years have witnessed the emergence of multicore microprocessor chips (CMPs) as a practical and expedited way of exploiting the potentials of increasing number of transistors within a chip. Snoop filter mechanism is explained by a common mechanism to ensure cache coherence is to issue snoop requests to all processors to check for the presence of cached data. As most of the snoop requests result in misses in caches and waste a huge amount of power, snoop filters are widely used to filter out unnecessary snoop requests to reduce power consumption. The energy saving's that results from the snoop filtering in this scheme proposed is around 30% across the benchmarks studied in both a quad-core design in 65 nm and 8-core design in the 45 nm CMOS.

III. RESULTS AND DISCUSSION

We have analysed that the portable electronic devices that contain microprocessors, in which battery weight and size is critical, but because of heat dissipation issues in larger desktop and parallel machines we see that removing the generated heat and the drive towards “green” computers are making power reduction a priority. Improvements in the cache organizations for higher performance commercial processors also serve to decrease the traffic on high capacitance buses. This clearly helps to save power although the primary goal is improving performance since we believe that low power architectures should be open to sacrificing some performance for power savings. We see that by the proposed technique snoop related energy dissipation is decreased by 30 % on the average benchmarks studied.

IV. CONCLUSION AND FUTURE SCOPE

This paper will conclude with the application of these metrics to quantify three important principles of energy-efficient microprocessor design. Also we have learnt that the use of filtering snoops in a multicore microprocessors has helped the industry of microprocessors to become more energy efficient over the years. An organized analytical approach to the optimization of power in microprocessor design, based on metrics that include the requirement of both throughput and energy, as well as actual application operation, allow the designer to quantify energy efficiency and provide insights into the design issues of energy efficient processor design. In-spite of the increasing commercial interest in the sophisticated embedded microprocessors, very little work has been conducted to improve the Energy Delay performance of embedded processor systems through architecture. Thus we can say that energy efficiency should not come at the cost or performance.

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