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Performance of Diagonal Mesh Network on Chip using NS2

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Abstract— Network on Chip (NoC) is an interconnection network, which provides a network architecture to overcome limitations of System on Chip(SoC). The Interconnection among multiple cores on a chip has a major effect on communication and performance of the chip in terms of latency and throughput. Many routing architectures and routing algorithm have been developed to alleviate traffic congestion, performance enhancement and low power consumption for Network on Chip(N0C). In this paper, Diagonal Mesh NoC architecture is described using Network Simulator (NS2), which reduces the load distribution across the network by reducing the diameter of the network, as a result, routing cost also reduces. In Diagonal Mesh topology, routing estimates the alternative routes with priority given to a diagonal path. In this paper, it is seen that latency reduces for a pair of nodes that uses the diagonal path as compared to another pair of nodes. Throughput is also enhanced by this approach.

Keywords— Network on Chip (NoC), Topology, Latency, Throughput, NS2.

I. INTRODUCTION

System on Chip (SoC) is complex and consist of heterogeneous IP cores. IP cores may be video processor, Image processor, programmable processors, memories, input /output interface, custom hardware, peripherals, external interface IP (INTELLECTUAL property) blocks. Due to the rapid progress in electronic systems, the number of cores in SoC has been increased to enrich the performance of the system. With the rising number of IP cores in SoC, many issues have arisen like poor Scalability, more power consumption, high complexity, high latency etc. the limitation of SoC are resolved by Network on Chip(NoC).
NoC is an interconnection network, which provides a network architecture to overcome limitations of SoC. In NoC network architecture and routing algorithm are important for enriching the performance of the system.

Before the advent of NoC interconnection architecture was based on dedicated wire and bus-based interconnections used for communicating with different IPs components. All the components in the SoC are communicating using a single transporting medium. This allows only one communication at a time managed by arbiter however when the number of components increases than the performance will degrade due to bandwidth limitation. In order to solve this restricted access problem, a full crossbar switch approach is used. As the number of integrated IPs increases wiring complexity also increases. The hierarchical bus system can be used to solve bandwidth limitation in the shared bus system. In this case, a bridge is used to connect two bus systems but here bridge hold-up access when two buses want to communicate between them which results in the increase of latency.

NoC has several merits such as high bandwidth, low latency, low power consumption and scalability as compared to dedicated wiring and shared bus.

A. NoC Description

The communication infrastructures based in NoC has Network Elements (NE) and Network Interfaces (NI). The packet travels across the Network Elements while the Network Interfaces provide an interface with the IP or Resource

The following are the main characteristic of NoC:

1. Topology: Arrangement of tiles and physical connectivity between them.
2. Switching: Allocating the path for data transfer from the inport to the outport.
3. Routing: Determines route for the message to transverse in the network.
4. Flow Control: Dynamic allocation of the channel
5. Buffering: It is the process of storing the packets when they cannot be processed.
6. Arbitration: Planning the use of channels and buffers.

B. Topology

Core, network interface, and router together form a tile. The arrangement of tiles and their interconnectivity leads to the formation of a Topology. Owing to their grid-type shapes and regular structure 2D mesh is the most appropriate for the two-dimensional layout on a chip [1]. A decent topology is one which offers less latency (hop count), more path diversity, high throughput and can support load balancing [2]. 2D Mesh is the most commonly used topology in commercial and industrial prototypes like Tilera multicore family or Intel 80 cores Polatis chip. But due to the constraint of 2D mesh, alternative topologies or modification to 2D mesh are projected [3]. Other standard NoC topologies are Torus, Folded Torus, Ring, Octagon, Star, SPIN (Scalable Programmable Integrated Network), Binary Tree(BT), Binary Fat Tree(BFT)and CLICHE [4]. The arrangement of these nodes in the chip affects the bandwidth and latency of the network [5].

Rest of the paper is organized as follows, Section I contains the introduction of Network on Chip, Section II contains the related work of NoC topology, Section III contains Architecture specification and performance, Section IV describes results and discussion for diagonal mesh topology and Section V concludes research work.

II. Related Work

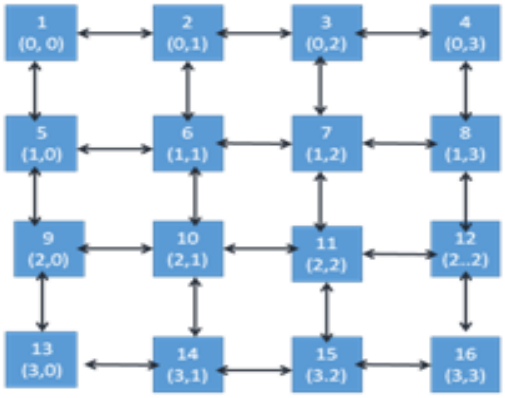

Figure 1: 2D Mesh Topology

Figure 1 shows a simple Mesh network that is commonly used in NoC because of its simplicity. Mesh topology suffers from shortcomings such as high power consumption and latency increase when the diameter of the network increases. To reduce latency, the diagonal concept is used which is demonstrated in Figure 2. For a packet to transverse from source to the destination, it requires two hops if horizontal(X) and vertical(Y) methodology is used but if the diagonal method is used then it requires only one hop. In diagonal conception, the number of hop count reduces as compared to XY method. Diagonal links restraint to less average latency than nondiagonal topology. Due to the advent of X-architecture routing technique, inchip manufacturing additional diagonal links to the 2D mesh network are possible [6].

In this paper, the diagonal Mesh topology for latency enhancement is explained.

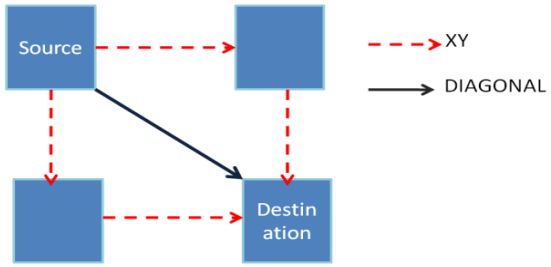

Figure 2: Diagonal concept

III. Methodology

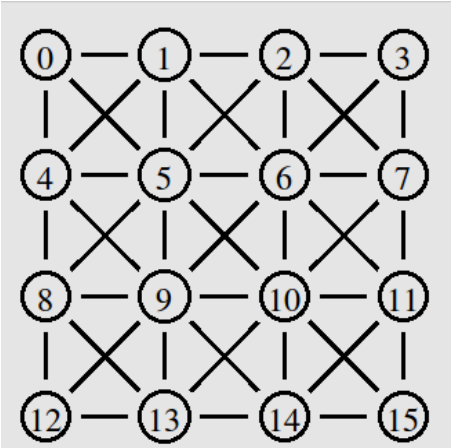

Figure 3. Diagonal Mesh network architectures

A. Architecture Specification

Figure 3 shows diagonal mesh topology. Each Diagonal Mesh tile that has a bidirectional port for communication with its neighbour router namely East(E), West(W), North(N), South(S), Northeast(NE), Northwest(NW), Southeast(SE) and Southwest(SW). Each corner tile has three neighbours, border tile has five neighbours and others have eight neighbours. Each router is identified by unique integer ID. Four diagonal links are added to basic Mesh. For an nxn topology node degree is 3 for a corner,5 for border and 8 for generic, Network diameter is n-1, Bisection bandwidth is 3n-1. Diagonal Mesh has more multiple paths for communication as compared to Mesh topology. Multiple paths help in the reduction of latency.

A node is represented by a circle as shown in Figure 3. It acts as a source or a destination and a router if it is an intermediate node. The node receives packets, and forwards them on the links specified by the router with the help of the

routing table or delivers them to the ports specified in the packet header [7]. A node in NS2 uses a flat-addressing and static routing by default [7]. The routing table is computed once at the beginning of the Simulation phase and does not change thereafter [7].

B. Architecture Performance Evaluation

A 4 x 4 Diagonal mesh topology is evaluated using Network Simulator (NS2). NS2 is an object-oriented open-source discrete event network simulator developed at UC Berkeley. NS2 is used to simulate real-time network traffic and topology for analysis. NS2 has been developed in C++ and TCL [7]. TCL programming is used for simulation and C++ is used for adding a new module. TCL is an interpreted language. Each instruction is a command in Tcl program. TCL programming is used to write simulation script in ns2. OTCL is an extension of TCL with the object-oriented feature. OTcl is short for MIT Object Tcl [7].

In NS2 "ns" command is used for execution of the file. After execution of the Tcl file through NS2, the output of a simulation is trace file. The simulation outputs provided by NS2 are either in text format or animation format. These outputs can be viewed by NAM tool and graphs can be obtained by the tool XGraph [7]. A scripting language AWK can be used to extract the necessary information from a trace file to grasp the network performance [7].

NAM provides many features for visualization. These features can be used for animating flow of various coloured packets, the positioning of nodes, colouring a precise connection, changing the shape of nodes colouring a specific link, and queue observing etc. [7]. Figure 3 shows a sample NAM window for a Diagonal Mesh topology with 16 nodes and Figure 4 shows the Diagonal Mesh network architectures scenario of packets roving from source to destination.

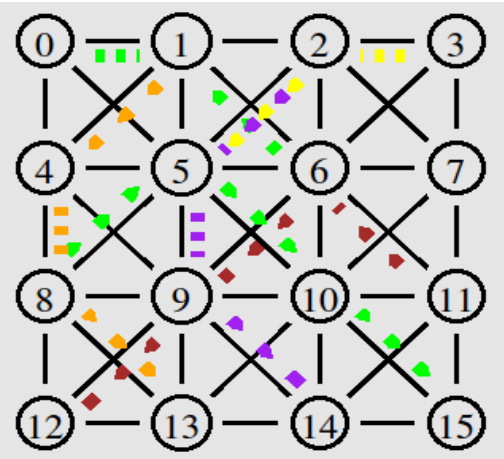

Figure 4. Diagonal Mesh network architectures scenario of packets roving from source to destination.

NS2 simulation consists of three main steps.

1. Design of topology is the most important step. Here 4 x 4 Diagonal Mesh topology is defined.
2. This step also includes configuring the simulation scenario by the various parameter applied in NS2 to the topology and running simulation of the design. Simulation parameters are listed in Table 1.
3. The final step in a simulation is to collect the result of the simulation and trace the simulation and writing AWK script.

Table 1. Parameters for simulation of Diagonal Mesh Topology

Parameters	Specifications
Number of nodes	16
Connection type	Router to Router
Protocol for transmission	UDP(User Datagram Protocol)
Routing Scheme	Static
Routing Protocol	Dijkstra shortest path
Bisection Bandwidth (Max.)	Router-to-router – 1Mb
Traffic Generation	CBR(Constant Bit Rate)
Traffic Rate	100 kb
Packet Size	500-200bytes

Performance evaluation parameters for Diagonal mesh topology are listed below.

1. Latency: Latency is the average delay between end to end delivery of packets. It is used to measure the performance of the network. It is expressed in simulator clock cycles. Latency is reduced by using diagonal paths since multiple paths are available for routing.

2. Throughput: Throughput is defined as the maximum traffic that the network can handle. It is measured in message/second or message/clock cycle. The normalized unit is bits per second of successful packet deliveries.

IV. RESULTS AND DISCUSSION

NS2 is used for simulation of a NoC topology. For understanding the behaviour of a NoC topology a 4×4 Diagonal Mesh, topology was simulated. Figure 2 illustrates Diagonal Mesh topology here router nodes are denoted by the circle and they are interconnected by bidirectional links. Table 1 shows various parameters applied for simulation.

The scenario of packet transversal from source to destination is mentioned in table 2. Here some links 2 to 5, 1 to 2 and 1 to 4 are shared between routers for communication to check the effect of latency. Latency and throughput plot for the above scenario is shown in Figure 5 and 6 respectively.

Latency is measured in milliseconds(ms) and throughput in kilobytes per second (Kbps). Node pair 8 to 15 and node pair 11 to 12 uses completely diagonal path for packet transverse so latency reduces for these pair of nodes as compared to another pair of nodes as seen from Figure 5.

Table 2. Packet transversal path from source to destination

Source	Destination	Path of transverse from source to destination
0	7	0,1,2,7
7	4	7,2,1,4
3	5	3,2,5
8	15	8,5,10,15
11	12	11,6,9,12
2	14	2,5,9,14
1	13	1,4,8,13
6	0	6,1,0

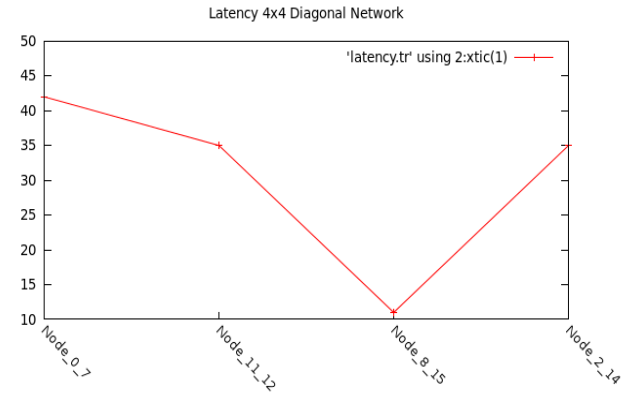

Figure 5. Latency of Diagonal Mesh network architectures

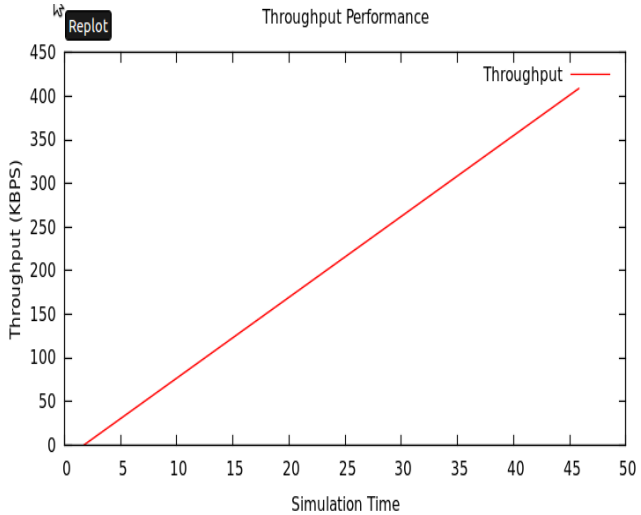

Figure 6. Throughput plot of Diagonal Mesh network architectures.

V. CONCLUSION

XY is a deterministic routing algorithm, hence the path taken by the packet for every source-destination pair is fixed. Hence Overall latency of the packets increases. In a diagonal Mesh topology, a diagonal route is given priority and it also offers multiple paths for transverse. For the Diagonal mesh topology of nxn, the shortest path from any source to destination is n-1, it means that shortest path is always less than n. Path 8,5,10,15 uses complete diagonal path so latency is reduced as seen from the Figure 5 latency plot. From Figure 6 it is observed that Throughput performance also increases. Hence Diagonal Mesh topology outpaces other topologies.

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Authors Profile

Ms.P.P.Papalkar pursed Bachelor of Engineering from University of Amravati, Amravati in 1992 and Master of Engineering from Shivaji University in year 2006. She is currently pursuing Ph.D. and currently working as Associate Professor in Department of Electronic and Communication, Ramrao Adik Institute of Technology, Navi Mumbai since 2007. Her main research work focuses on Image processing and Network on chip. She has 13 years of teaching experience and 5 years of Research Experience.

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